Session 17: Characterization, Reliability, and Yield - Innovative Characterizations
Tuesday, December 4, 9:00 AM
Plaza B
Co- Chairs: K. Okada, TowerJazz Panasonic Semiconductor
K. P. Cheung, NIST

9:05 AM - 9:30 AM
17.1 Characterization Methodology and Physical Compact Modeling of in-Wafer Global and Local Variability, *K. Pradeep, T. Poiroux**, P. Scheer, A. Juge, G. Gouget, and G. Ghibaudo*, STMicroelectronics, *IMEP-LAHC, MINATEC Campus, **CEA-LETI*

A unified, industrially compatible methodology to characterize and model in-wafer variability at different spatial scales, with addressable array test structures is proposed. Using a physics-based compact model, a single statistical model for both local and global variability is developed for the first time. The proposed method and model are validated using 28 nm FD-SOI devices and the dependence of dominant sources of variability on bias and device geometry is evaluated.

9:30 AM - 9:55 AM
17.2 Too Noisy at the Bottom? -Random Telegraph Noise (RTN) in Advanced Logic Devices and Circuits (Invited), *R. Wang*, S. Guo, Z. Zhang, Q. Wang*, D. Wu*, J. Wang*, R. Huang, Peking University, *Synopsys, Inc.*

In this paper, the recent advances of our studies on RTN are presented from device, circuit, and EDA perspectives. RTN characteristics in FinFETs are investigated and compared with planar devices. The AC RTN effect is discussed for understanding RTN impacts in practical circuit applications. Then, a new and efficient circuit simulation platform for RTN is presented for the first time, which has been implemented in HSPICE using OMI/TMI. In addition, some open questions related to RTN are discussed with outlooks.

9:55 AM - 10:20 AM
17.3 Comprehensive Study on the "Anomalous" Complex RTN in Advanced Multi-Fin Bulk FinFET Technology, *J. Zhang, Z. Zhang, R. Wang, Z. Sun**, Z. Zhang, S. Guo, R. Huang, Peking University, *National Key Laboratory of Science and Technology on Micro/Nano Fabrication, **Fuzhou University*

In this paper, random telegraph noise (RTN) in advanced multi-Fin bulk FinFETs are comprehensively studied for the first time. Based on the statistical experiments, the complete categories of simple and complex RTNs are identified and analyzed in details. Especially, the anomalous ""reversal RTN"" induced by 2 metastable states in single oxide trap, are found not rare, but appears at a certain percentage, which provides a unique opportunity for statistically studying the metastable states directly from RTN measurements. In addition, anomalous layout dependence of RTN amplitudes are observed, with respects to Fin number. The results are helpful for deep understanding of reliability physics and robust circuit design against RTN.

10:20 AM - 10:45 AM
17.4 An Unique Methodology to Estimate The Thermal Time Constant and Dynamic Self Heating Impact for Accurate Reliability Evaluation in Advanced FinFET Technologies, *S. Mukhopadhyay, A. Kundu, Y.W. Lee, H. D. Hsieh, D.S.Huang, J.J.Horng, T.H.Chen, J.H. Lee, Y.S. Tsai, C.K.Lin, R. Lu, and J. He, Taiwan Semiconductor Manufacturing Company Limited*

The increasing impact of self-heating effect (SHE) in complex FinFET structure is a serious reliability concern. Although the evaluation of SHE has become extremely arduous; this work proposes an in-situ

layout based experimental solution to find out the precise thermal time constant (TTH) due to SHE on advanced FinFET devices, even with the application of very pragmatic 'circuit-like' gate and drain input waveforms. Using this precise TTH, the accurate dynamic thermal profile is found out from SPICE simulations. Finally, the true degradations due to different reliability mechanisms are evaluated including SHE impact and successfully compared with measured FinFET silicon data.

10:45 AM Coffee Break

11:10 AM - 11:35 AM

17.5 7nm FinFET Plasma Charge Recording Device, *Y.-P. Tsai, J-R Shih*, Y-C King and C. J. Lin, National Tsing Hua University (NTHU), *Taiwan Semiconductor Manufacturing Company*

A new wafer-level coupling plasma charge recorder fabricated with 7nm FinFET CMOS logic process is presented in this paper. This plasma ion charge recording device provides the historic and quantitative plasma ion charges of damascene metallization steps in advanced 7nm FinFET COMS logic processes. The high-resolution plasma ion recorder is formed by an accurate FinFET coupling structure to store the plasma ion level and distribution of the whole wafer. By a simple wafer-level WAT measurement, the promising plasma charge recording device can efficiently collect the accumulated ion charges, ion polarization, and tiny plasma fluctuation of each metallization process step in 7nm FinFET CMOS logic technologies, which definitely provides a superior device and method in developing a reliable and non-latent plasma damage process for 7nm FinFET technology and beyond.

11:35 AM - 12:00 PM

17.6 Development of X-ray Photoelectron Spectroscopy under bias and its application to determine band-energies and dipoles in the HKMG stack, *P. Kumar, C. Leroux*, F. Domengie, E. Martinez*, V. Loup*, D. Guiheux, Y. Morand*, J-M Pedini*, C Tabone*, F. Gaillard*, G. Ghibaudo**, STMicroelectronics, *Univ. Grenoble Alpes, CEA, LETI, **IMEP-LAHC, Minatec/INPG*

In this paper, we present for the first time specific methodology and test structures authorizing an accurate analysis of XPS under bias measurements. Such analysis which identifies effective biasing across the device, allows to determine the absolute energy levels of the different layers in the HKMG stack at any bias. This enables an accurate band diagram identification and it is applied to analyze the physical mechanisms at work in the threshold voltage (VT) engineering of HKMG stacks. We demonstrate that VT shift induced by La and Al additives or metal gate thickness variations originates by the modifications of the dipole at SiO2/high-k interface.

12:00 PM - 12:25 PM

17.7 In-situ investigation of the impact of externally applied vertical stress on III-V bipolar transistor, *Y. Liu, G. Hiblot, M. Gonzalez, K. Vanstreels, D. Velenis, M. Badaroglu**, G. Van der Plas, I. De Wolf, imec, *KU Leuven, **Qualcomm Inc*.

This work presents a new methodology to investigate in-situ the impact of vertical stress on the electrical characteristics of semiconductor devices. It is applied for the first time on III-V Heterojunction Bipolar Transistors (HBT). It combines a nanoindenter, which is used to apply controlled vertical forces on the sample surface, with in-situ electrical measurements using micro probes. The HBT devices are shown to be significantly affected by vertical stress: both the current and the capacitance show a reduction with increasing compressive vertical stress. The observations are confirmed by TCAD simulations. This method can be employed to extract the sensitivity of advanced devices to vertical (out-of-plane stress) which is a growing concern in packaging and 3D integration.