In this short course, we invite world’s leading experts to give us their vision on what’s needed for future CMOS technology to scale to 5 nm and beyond. 5 nm is within a factor of ten of the atomic size, which demands a paradigm shift in many aspects of the technology: device type, process integration, interconnect, patterning, and manufacturability.

For device and material options, III-V MOSFETs, band-to-band tunnel FETs, nanowire FETs, and 2D semiconductors will be considered, among other options. Their merits and challenges, with reference to today’s state-of-the-art 14 nm FinFETs, will be discussed. For process integration, the focus is on scaling of fully depleted devices, FinFETs, high-mobility channel material, and SRAM cell. Opportunities include horizontal and vertical nanowires with 3D integration. Interconnects will face power dissipation, insufficient bandwidth, and signal latency problems. The question is how far can we push Cu/low-k to its physical limitation? And will alternative schemes, like carbon nanotubes, optical interconnects, and 3D interconnects meet the challenge? Patterning at 5 nm and beyond will be extremely demanding, requiring a multiplex of resolution enhancing techniques and extreme ultra-violet lithography whose status will be reviewed. Challenges on the resist and mask will also have to be met. Variability is the maker or breaker of CMOS manufacturing at 5 nm. Various sources of local, global, and time dependent variability will be examined. Design-technology co-optimization (DTCO) will be discussed as one of the possible solutions. The short course will conclude with a few thoughts from the organizer on the historical perspective.

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