High Electron and Hole Mobility Enhancements in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator

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Fully depleted MOSFETs were fabricated on strained Si/strained SiGe (46% Ge)/strained Si heterostructures on insulator (HOI) for the first time, demonstrating both high electron and hole mobility enhancements while maintaining excellent subthreshold characteristics. The total thickness of the heterostructure on insulator is less than 25 nm. At an inversion charge density of 1.5×10^{13} cm^{-2}, mobility enhancements of 90% and 107% are obtained for electrons and holes respectively. We demonstrate the mobility scaling of HOI structures with Si cap thickness and compare to new results for 14 nm-thick 1.67% Strained Silicon Directly on Insulator (40% SSDOI).

SSDOI provides benefits for both electrons and holes [1-3], but requires strain levels equivalent to 40% Ge to obtain hole mobility enhancement at high inversion charge density N_{inv}. Bulk dual-channel MOSFETs (strained Si/strained $Si_{1-z}Ge_z$ on relaxed $Si_{1-y}Ge_y$ virtual substrates, $y<z$) [4] have higher hole mobilities than SSDOI at high N_{inv}, even for lower Ge content of the relaxed virtual substrate and at lower strain levels. However, degraded subthreshold characteristics and increased junction leakage remain problems for such structures [5]. With HOI, these problems are eliminated and the benefits of the high-hole-mobility buried channel are merged with the advantages of fully depleted strained Si on insulator.

HOI and SSDOI were fabricated by a bond and etch-back technique (Fig. 1) [3]. Graded $Si_{1-x}Ge_x$ relaxed layers, and device layers were grown in an Applied Materials "Epi Centura" system. The LPCVD oxide was planarized prior to bonding and layer transfer. By wet etching, all but the strained Si cap layer (electron channel), compressively strained $Si_{1-z}Ge_z$ hole channel, and strained Si interfacial layer were removed. The bottom Si layer is included to minimize Ge at the buried oxide interface, different from prior work [6,7]. The band structure (Fig. 2) is such that electrons will populate the Si cap, and holes populate the buried channel and/or the Si cap. In Fig. 2, the experimental splits are defined. The Si tensile strain level (determined by y) and buried channel z were varied.

A range of cap thicknesses was prepared. 2D device simulations were performed to fit the experimental gate to channel capacitance to extract the Si cap thickness (Fig. 3). Quantum effects were taken into account by using the density gradient quantum correction model with the Dessis default parameters [8,9]. The buried channel inverts prior to the Si cap channel, resulting in a characteristic "hump", which gradually disappears as the cap is thinned.

An advantage of thin-body HOI over bulk dual channel MOSFETs is the improved subthreshold slope (SS). For both n- and p-MOSFETs SS=66-70 mV/dec. for a thermally grown ~4 nm-thick gate oxide (Fig. 4). Fig. 5 shows low SS independent of cap thickness in the range of 2 to 7 nm, a dramatic improvement over bulk dual-channel p-MOSFETs [5]. Electron mobilities agree with results for SSDOI [3] with enhancements of 75-90% compared to the universal mobilities (Fig. 6). For hole mobility (Fig. 7), the dual-channel structure is important. As Ge content is increased from 35 to 46% the mobility is improved considerably, for constant Si cap thickness. In particular at high N_{inv}, measurements indicate the possibility to scale mobility by decreasing the Si cap thickness. To understand this, the hole distribution at $N_{inv}= 10^{13}$ cm^{-2} was simulated for three cap thicknesses (Fig. 8). For the thinnest cap (1.7 nm), inversion occurs only in the SiGe buried channel, where mobility is higher. Mobility scales similarly with cap thickness for split A: 46/24 and B: 46/30 (Fig. 9), but due to the higher level of compressive strain of the buried channel in split A, the mobility is higher for the range of cap thicknesses studied. Mobility is improved by 35% at $N_{inv}= 10^{13}$ cm^{-2} as the cap is reduced from 7 to 2 nm. We also confirm that mobility scaling with cap thickness is most effective at high N_{inv} (higher field), where the surface channel degrades the thick cap devices (Fig. 10).

Finally, we compare the HOI mobilities from Fig. 7 with those of new results for 40% SSDOI shown in Fig. 11, the highest hole mobilities reported for SSDOI to date. Fig. 12 compares the HOI and SSDOI to the Si reference [9]. The enhancements are 110% for the 2 nm thick cap HOI and 70% for 40% SSDOI at $N_{inv}=10^{13}$ cm^{-2}. Comparing HOI hole mobilities to that of the 40% SSDOI (Fig. 13), HOI offers more enhancement at both low and high N_{inv} than 40% SSDOI, due to the high-hole-mobility channel.

In summary, we have demonstrated thin-body n- and p-MOSFETs on a strained heterostructure on insulator, with excellent subthreshold characteristics. The structure merges benefits of a FD-SOI technology with the mobility advantage of a high [Ge] buried hole channel, while maintaining high electron mobility enhancement.

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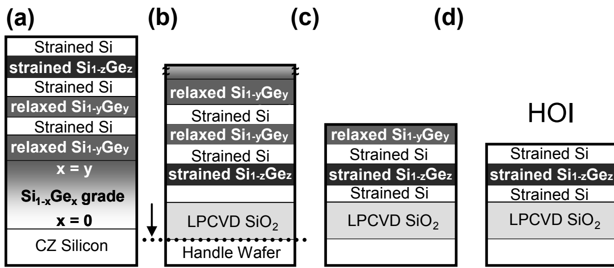

Fig. 1 The HOI fabrication process: (a) the as grown structure (b) deposition of oxide, flip, bond (arrow marks bond interface), grind back, and TMAH etch. (c) acetic acid based etch until Si etch stop, remove etch stop (d) SC-1 remove 150 nm SiGe leaving HOI structure.

	A	B	C
y	0.24	0.30	0.24
z	0.46	0.46	0.35
y	0.24	0.30	0.24

Fig. 2 The HOI band structure. Holes populate the buried 12 nm thick $Si_{1-z}Ge_z$ channel and/or the strained Si surface channel in inversion, whereas electrons populate only the strained Si. The three experimental splits are defined in the table.

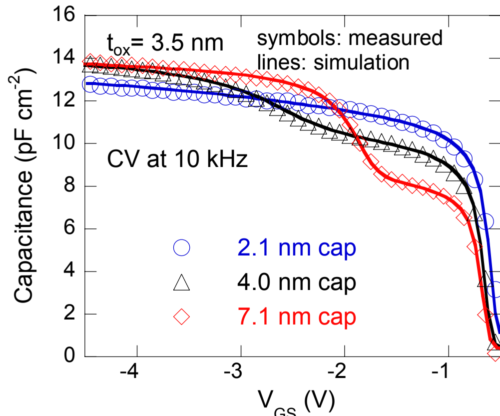

Fig. 3 Gate to channel inversion capacitance for HOI. The strained Si cap thickness was extracted by fitting experimental gate to channel capacitance to simulations [8,9]. The "hump" is due to inversion of the buried channel.

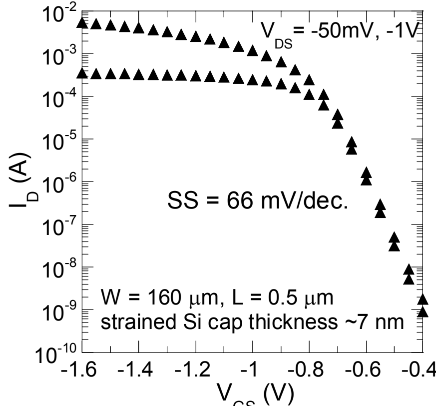

Fig. 4 I_D-V_{GS} characteristics showing the subthreshold region. Both N and NMOS had SS ~ 66-70 mV/dec. N+ poly-Si gates were used for both n- and p-MOSFETs.

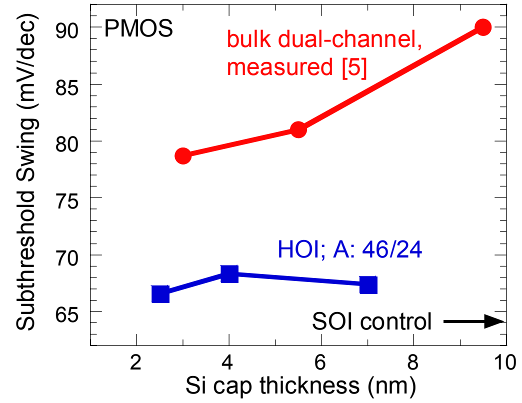

Fig. 5 Subthreshold characteristics vs. Si cap thickness for HOI. The measured HOI subthreshold slope (SS) is independent of strained Si cap thickness (fully depleted film), an improvement compared to measured bulk dual-channel results [5].

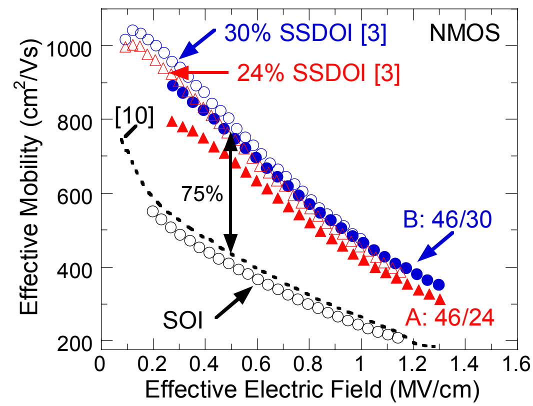

Fig. 6 NMOS effective mobility as a function of E_{eff}. $\mu_{eff}=L/W*I_D/(Q_{inv}V_{DS})$ was extracted by integration of C_{GC}, measuring I_D at an applied V_{DS}=50mV. A mobility extraction device was used to reduce the influence of series resistance on the extracted mobility [3]. The universal mobility is indicated [10].

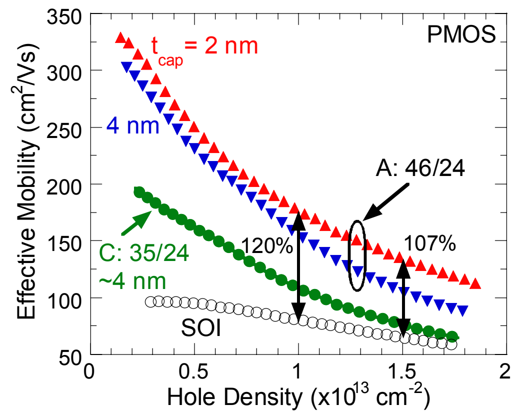

Fig. 7 PMOS effective mobility as a function of N_{inv}. The enhancement compared to the SOI control at N_{inv}= $1x10^{13}$ cm^{-2} is 120%. As the Ge content of the buried channel is increased (keeping the cap thickness constant), the mobility is increased. For a given structure (z=0.46, y=0.24), a thinner cap enhances the mobility.

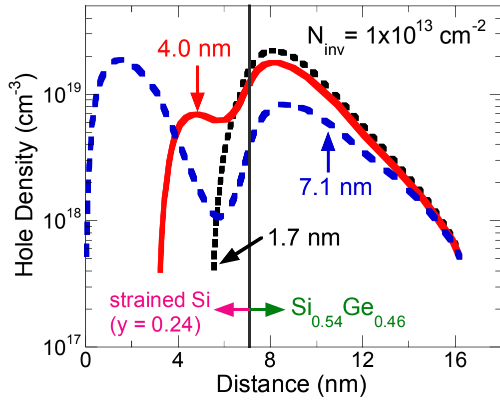

Fig. 8 Simulation of the hole distribution between the strained Si cap (left part of the figure) and the high-hole-mobility buried channel (right) for three cap thicknesses. At N_{inv}= 1x10^{13} cm^{-2} and for a 7.1 nm thick cap, the holes populate mainly the strained Si surface channel. For the thinnest cap, holes are in the buried $Si_{1-z}Ge_z$ layer.

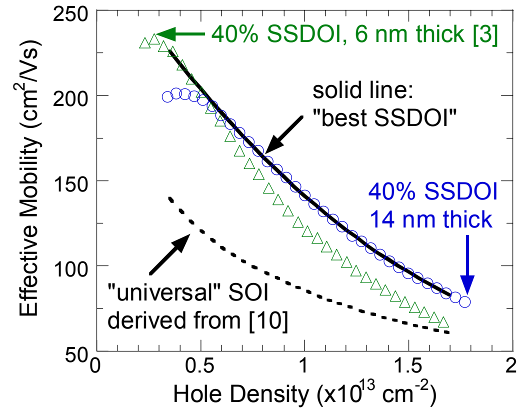

Fig. 11 Hole mobility for 40% SSDOI. 14 nm thick SSDOI has high mobility enhancement even at high N_{inv}. The highest 40% SSDOI mobility results to date were fit to create a "best SSDOI" curve to serve as a reference (Fig. 13). We derived a "universal" SOI mobility curve from [10].

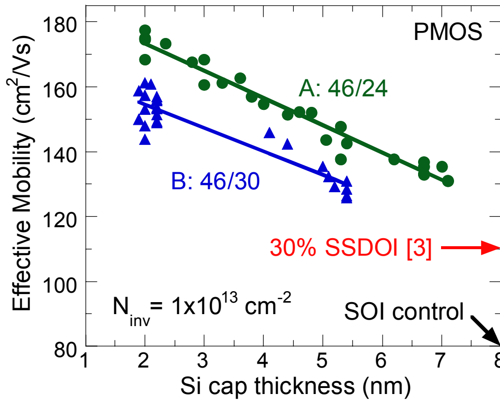

Fig. 9 Hole mobility vs. Si cap thickness. For each device, the cap thickness was extracted by CV analysis (Fig. 3). Mobility is enhanced as the Si cap is thinned. The trend is similar for the A and B splits. Due to the larger strain level for the A split, the mobility is larger.

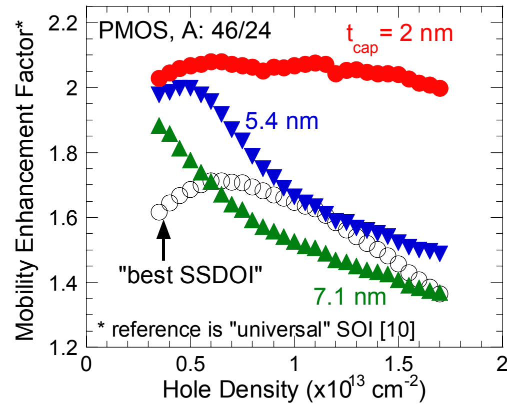

Fig. 12 The mobility enhancement factor of HOI split A: 46/24 and the best 40% SSDOI curve (Fig. 11) relative to the "universal" SOI mobility, derived from [10]. The 2 nm thick cap HOI has a mobility enhancement factor of 2.1X independent of N_{inv}.

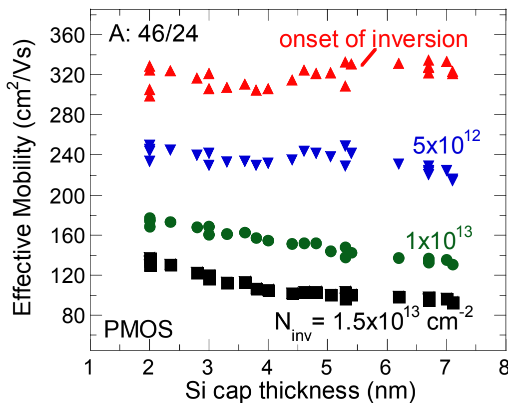

Fig. 10 Hole mobility vs. Si cap thickness. At low N_{inv}, holes populate only the buried channel (mobility independent of cap thickness). At high N_{inv}, mobility decreases with increasing Si cap thickness, due to inversion in the strained Si surface channel.

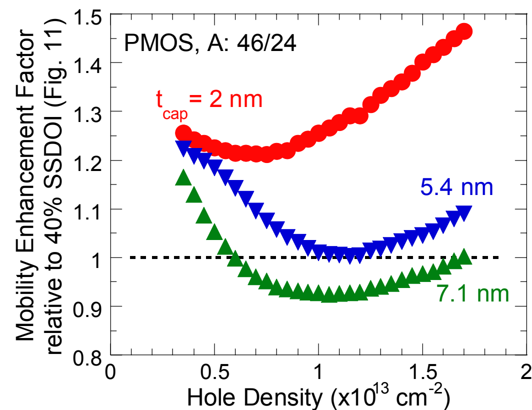

Fig. 13 Enhancement factor for HOI split A relative to the best 40% SSDOI (Fig. 11). HOI offers more enhancement than 40% SSDOI at both low and high N_{inv} due to the high-hole-mobility buried channel. To achieve a mobility advantage in HOI compared to SSDOI, cap thicknesses of < 5 nm are required.