Session 7: Modeling and Simulation – Modeling Simulation of Extremely Scaled Group IV and III-V FETs
Monday, December 15, 1:30 p.m.
Imperial Ballroom A
Co-Chairs: Jeff Wu, TSMC
Herve Jaouen, STMicroelectronics

1:35 p.m.
7.1 Impact of 3D Integration on 7nm High Mobility Channel Devices Operating in the Ballistic Regime, W. Guo, M. Choi*, A. Rouhi, V. Moroz*, G. Van der plas, P. Absil and E. Beyne, IMEC, *Synopsys, Inc.

We report for the first time the impact of 3DIC process induced local thermo-mechanical stress effects on CMOS devices for 7nm technology node (N7). The impact is smaller but has new dependencies with respect to the device operation, ballistic current ratio and the channel material considered.

2:00 p.m.
7.2 A Mobility Enhancement Strategy for sub-14nm Power-efficient FDSOI Technologies, B. De Salvo, P. Morin*, M. Pala**, G. Ghibaudo**, O. Rozeau, Q. Liu*, A. Pofelski*, S. Martini, M. Cassé, S. Pilorget*, F. Allibert^, F. Chafik*, R.G. Southwick**, D. Chanemougame*, L. Grenouillet, K. Cheng***, F. Andrieu, S. Barraud, S. Maitrejean, E. Augendre, H. Kothari*, N. Loubet*, W. Kleemeier*, M. Celik*, O. Faynot, M. Vinet, R. Samspon*, and B. Doris***, CEA-LETI, *STMicroelectronics, **IMEP, ***IBM, ^SOITEC

In this paper, we present an original multi-level evaluation methodology for stress engineering device design of next-generation power-efficient devices. FDSOI is chosen as ideal test vehicle, as it offers the advantage of sustaining significant stress within the channel without plastic relaxation (the thin channel staying below the critical thickness [2]). Starting from 3D mechanical simulations and piezoresistive coefficient data, an original, simple, physically-based model for holes/electrons mobility enhancement in strained devices is developed. The model is calibrated on physical measurements and electrical data of state-of-the-art devices. NEGF quantum simulations of stress-enhanced mobility give physical insigths into mobility behavior at large stress (~3GPa). Finally, the new strained-enhanced mobility model is introduced in an industrial compact model [3] to project evaluation at the circuit level. Ring oscillator simulations showed that a dynamic power gain of 50% could be achieved while maintaining circuit frequency performance thanks to the use of efficient mobility boosters. By means of a multi-scale modelling validated on measurements, a clear scaling path to achieve high mobility, power-efficient sub-14nm FDSOI technologies has been identified.

2:25 p.m
7.3 Coupled Monte Carlo Simulation of Transient Electron-Phonon Transport in Small FETs, Y. Kamakura, I.N. Adisusilo, K. Kukita, G. Wakimura, S. Koba**, H. Tsuchiya* and N. Mori, Osaka University, *JST-CREST, **Kobe University

Using a coupled MC technique for solving both electron and phonon Boltzmann transport equations, the transient electrothermal simulation of nanoscale FETs is carried out. It is shown that the time constants for the electron and phonon transport are different in order of magnitude, and the self-heating showed little impact on digital circuit delay. On the other hand, it would affect the BTI reliability because of the long decay time of the created hot spot.

2:50 p.m.
7.4 Modeling and Optimization of Group IV and III-V FinFETs and Nano-Wires, V. Moroz, L. Smith, J. Huang, M. Choi, T. Ma, J. Liu, Y. Zhang, X.-W. Lin, J. Kawa and Y. Saad, Synopsys, Inc.

Comparative analysis of group IV and III-V 7nm HP/SP/LP FinFETs. Mechanical stability of fins drives transistor architecture choices. Benchmarking two-input NAND library cells based on quadruple patterning Si 7nm FinFETs, Ge SOI 7nm FinFETs, and EUV+DSA Si 5nm vertical nanowires exhibits 4x performance advantage of the 5nm vertical nanowire technology.

3:15 p.m.
7.5 Performance Evaluation of InGaAs, Si, and Ge nFinFETs Based on Coupled 3D Drift-Diffusion/Multisubband Boltzmann Transport Equations Solver, S. Jin, A.-T. Pham, W. Choi, Y. Nishizawa*, Y.-T. Kim**, K.-H. Lee**, Y. Park** and E. S. Jung**, Samsung Semiconductor Inc., *Samsung R&D Institute Japan, **Samsung Electronics

We present a simulation study of InGaAs, Si, and Ge nFinFETs by solving the coupled drift-diffusion and the multisubband Boltzmann equations solver in 3D domains. A few important improvements on the modeling of the surface roughness scattering, the density-gradient calibration, and the band-to-band tunneling are also shown.

3:40 p.m.
7.6 Simulation Analysis of III-V *n*-MOSFETs: Channel Materials, Fermi Level Pinning and Biaxial Strain, E. Caruso, D. Lizzit, P. Osgnach, D. Esseni, P. Palestri and L. Selmi, University of Udine

In this work we employ a state-of-the-art Multi-Subband Monte Carlo simulator to investigate the performance of III-V n-MOSFETs at LG=11 nm. We analyze GaSb versus InGaAs channel materials, electrostatic and transport implications of Fermi level pinning, strain induced effective mobility and on-current improvements and possible links to Fermi level pinning.

4:05 p.m.
7.7 Assessment of Hole Mobility in Strained InSb, GaSb and InGaSb Based Ultra-Thin Body pMOSFETs with Different Surface Orientations, P. Chang, X. Liu, G. Du and X. Zhang, Peking University

This work presents a systematic assessment of hole mobility in InSb, GaSb and InGaSb based ultra-thin body (UTB) double-gate (DG) pMOSFETs employing a self-consistent method based on 8×8 k•p Schrödinger and Poisson equations and Kubo- Greenwood formalism accounting for various scattering mechanisms. The results are validated against experiments. The effect of body thickness, surface/ channel orientation, biaxial- and uniaxial-strain on hole mobility have been investigated. For all of these materials with both unstrained and strained cases, (110)/[$1\bar{1}0$] is the optimal surface channel directions. In unstrained case, hole mobility of InSb/GaSb is high than that of Ge with μ_h(InSb) approaching 1118cm^2/Vs. Compressive strain can enhance hole mobility, the enhancement is 5.1× with 2GPa uniaxial comp. strain in InSb. For $In_xGa_{1-x}Sb$ QW HFET, enhancement is 2.4× with 2.55% biaxial comp. strain due to lattice mismatch with x=0.5, and can be optimized by TB and cap layer.