Session 6: Memory Technology – Resistive RAM
Monday, December 15, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Joshua Yang, Hewlett Packard Laboratories
Pawan Singh, Spansion

1:35 p.m.
6.1 Controling Oxygen Vacancies in Doped Oxide Based CBRAM for Improved Memory Performances, G. Molas, E. Vianello, F. Dahmani*, M. Barci, P. Blaise, J. Guy, A. Toffoli, M. Bernard, A. Roule, F. Pierre, C. Licitra, B. De Salvo and L. Perniola, CEA LETI Minatec, *Altis Semiconductor

Abstract— In this paper the concept hybrid CBRAM assisted by oxygen vacancies is presented for the 1st time. Doping the resistive layer of oxide/Cu based CBRAM with various dopant species and concentrations is proposed in order to improve the memory performances. By means of experimental characterizations, numerical model and atomistic calculations, we demonstrate that increasing the doping content ease the filament formation by facilitating the Cu injection in the resistive layer. The proper choice of the doping element and concentration allows to significantly reduce the forming voltage (up to a forming free behavior), or alternatively to increase the memory window of 3 decades, with no forming voltage increase and retention degradation (stable behavior at 200°C, 260°C soldering sustained).

2:00 p.m.
6.2 Process Integration of a 27nm, 16Gb Cu ReRAM, J. Zahurak, K. Miyata, M. Fischer, M. Balakrishnan, S. Chhajed, D. Wells, H. Li, A. Torsi, J. Lim, M. Korber, K. Nakazawa*, S. Mayuzumi*, M. Honda*, S. Sills, S. Yasuda*, A. Calderoni, B. Cook, H. Tran, B. Wang, C. Cardon, K. Karda, J. Okuno*, A. Johnson, T. Kunihiro*, J. Sumino*, M. Tsukamoto*, K. Aratani*, N. Ramaswamy, W. Otsuka*, and K. Prall, Micron Technology Inc., *Sony Corporation

A 16Gb NV ReRAM chip is fabricated at the 27nm node. 133MB/s Write and 666MB/s read performance is enabled. Architecture is 6F2 and utilizes highly modified BRAD access devices coupled with novel, self aligned plugs contacting a Damascene Cu-ReRAM Cell. Line-SAC Digit Lines running over the cell complete M-Bit formation.

2:25 p.m
6.3 Resistive Memories for Ultra-Low-Power Embedded Computing Design, E. Vianello, O. Thomas, G. Molas, O. Turkyilmaz, N. Jovanović, D. Garbin, G. Palma, M. Alayan, C. Nguyen, J. Coignus, B. Giraud, T. Benoist, M. Reyboz, A. Toffoli, C. Charpin, F. Clermidy and L. Perniola, CEA-Leti

Resistive memories (ReRAMs) are emerging as leading candidates to replace conventional Flash memories due to their high density, good scalability and low voltage. However, using ReRAM for embedded computing is still a futuristic goal. Depending on the application different ReRAM specifications are required. This paper addresses two technologies as an example of optimized devices for Ultra Low Power (ULP) FPGA and fixed-logic IC design. A Conductive Bridge RAM (CBRAM) cell with dual-layer electrolyte stack leads to a resistance ratio higher than 6 orders of magnitude and projected 10 years read disturb immunity at 0.04 V. This technology allows achieving dense memory configuration and solving FPGA leakage issue. An HfO_2/Ti based OxRAM cell presents a switching time lower than 10ns at 1V and a high endurance up to 1000M cycles. Thanks to low voltage and high speed this technology enables non-volatile Flip-Flop design, unifying non-volatility, zero standby leakage, and rapid power on/off operations for fixed-logic IC design.

2:50 p.m.
6.4 Point Twin-bit RRAM in 3D Interweaved Cross-point Array by Cu BEOL Process, Y.-W. Chin, S.-E. Chen, M.-C. Hsieh, T.-S. Chang*, C.J. Lin and Y.-C. King, National Tsing Hua University, *Taiwan Semiconductor Manufacturing Company

A self-rectifying twin-bit RRAM in a novel 3D interweaved cross-point array has been proposed and demonstrated in 28nm CMOS BEOL process. With TaO_x RRAMs on both sides of a single Via, the twin-bit RRAM cell is composed by Cu back-end layers only. Excellent selectivity by its asymmetric IV characteristic enables the twin-bit 1R cells to be efficiently stacked in 3D cross-point arrays.

3:15 p.m.
6.5 Experimental and Theoretical Understanding of Forming, SET and RESET Operations in Conductive Bridge RAM (CBRAM) for Memory Stack Optimization, J. Guy, G. Molas, P. Blaise, C. Carabasse, M. Bernard, A.

Roule, G. Le Carval, V. Sousa, H.. Grampeix, V. Delaye, A. Toffoli, J. Cluzel, P. Brianceau, O. Pollet, V. Balan, S. Barraud, O. Cueto, G. Ghibaudo, F. Clermidy, B. De Salvo and L. Perniola, CEA, LETI

In this paper, we deeply investigate for the 1st time the impact of the CBRAM memory stack on the Forming, SET and RESET operations. Kinetic Monte Carlo simulations (KMC), based on inputs from ab-initio calculations and taking into account ion hopping and chemical reaction dynamics are used to analyse experimental results obtained on decananometric devices. We propose guidelines to optimize the CBRAM stack, targeting Forming voltage reduction, improved trade-off between SET speed and disturb immunity (time voltage dilemma) and window margin increase (RESET efficiency).

3:40 p.m.
6.6 Ultrathin (~2nm) HfO_x as the Fundamental Resistive Switching Element: Thickness Scaling Limit, Stack Engineering and 3D Integration, L. Zhao, Z. Jiang, H.-Y. Chen, J. Sohn, K. Okabe, B. Magyari-Köpe, H.-S. P. Wong and Y. Nishi, Stanford University

This paper addresses the thickness scaling limit of HfO_x-based RRAM by a combination of theoretical calculations of electron transport and experimental demonstration of 2nm-HfO_x devices. The comparison of 2nm devices with thicker references and bilayer stacks confirm the switching thickness is less than 2nm. The 3D integration of 2nm-HfO_x devices enables much larger array size and leads to superior performances compared to planar devices.

4:05 p.m.
6.7 3D-stackable Crossbar Resistive Memory Based on Field Assisted Superlinear Threshold (FAST) Selector, S.H. Jo, T. Kumar, S. Narayanan, W.D. Lu and H. Nazarian, Crossbar Inc.

We report the integration of 4Mb 3D-stackable 1S1R passive crossbar RRAM arrays. Excellent selector performance is presented such as sharp switching slope of < 5mV/dec., selectivity of 10^{10}, and > 10^8 cycling. The integrated 4Mb 1S1R crossbar array offers >100 memory on/off ratio with less than 0.1nA sneak current.

4:30 p.m.
6.8 High-Drive Current (>1MA/cm^2) and Highly Nonlinear (>10^3) TiN/Amorphous-Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance, L. Zhang, B. Govoreanu, A. Redolfi, D. Crotti, H. Hody, V. Paraschiv, S. Cosemans, C. Adelmann, T. Witters, S. Clima, Y.-Y. Chen, P. Hendrickx, D.J. Wouters, G. Groeseneken and M. Jurczak, imec, *KU Leuven

Although several reported resistive switching structures show excellent memory characteristics, implementation of high-density Resistive RAM arrays lags behind, mainly due to the sneak currents issues. To suppress the leakage paths, a non-linear two-terminal selection device is required to connect serially with each resistive switching element in a 1S1R cell. In this work, we propose an optimized TiN/amorphous-Si/TiN MSM bidirectional two-terminal selector for high density RRAM arrays. The devices show superior performance with a high drive current exceeding 1MA/cm^2 and half-bias nonlinearity of 1500. Performance improvement is achieved by device and process engineering. Excellent reliability is fully demonstrated on 40nm-size crossbar structures, with statistical ability to withstand bipolar cycling of over 10^6cy at drive current conditions and thermal stability of device operation exceeding 3h/125^{0}C. Furthermore, for the first time, we address the impact of selector variability in a 1S1R memory array, by including circuit simulations in a Monte Carlo loop and point out the importance of selector variability for the low resistive state and its implications on the read margin and power consumption.