Session 35: Modeling and Simulation – Compact Modeling
Wednesday, December 17, 1:30 p.m.
Imperial Ballroom A
Co-Chairs: Andries Scholten, NXP Semiconductors
Roza Kotlyar, Intel

1:35 p.m.
35.1 A Physics-based Compact Model for FETs from Diffusive to Ballistic Carrier Transport Regimes, S. Rakheja, M. Lundstrom* and D. Antoniadis, Massachusetts Institute of Technology, *Purdue University

The virtual source (VS) model provides a simple, physical description of transistors that operate in the quasi-ballistic regime. Through comparisons to measured data, key device parameters can be extracted. The VS model suffers from three limitations: i) it is restricted to short channels, ii) the transition between linear and saturation regions is treated empirically, and iii) the injection velocity cannot be predicted, it must be extracted by fitting the model to measured data. This paper discusses a new model, which uses only a few physical parameters and is fully consistent with the VS model. The new model: i) describes both short and long channel devices, ii) provides a description of the current at any drain voltage without empirical fitting, and iii) predicts the injection velocity (device on-current). The accuracy of the model is demonstrated by comparison with measured data for III-V HEMTs and ETSOI Si MOSFETs.

2:00 p.m.
35.2 A Physics-Based RTN Variability Model for MOSFETs, M. Banaszeski da Silva, H. Tuinhout, A. Zegers-van Duijnhoven, G.I. Wirth* and A. Scholten, NXP Semiconductors, *UFRGS – Porto Alegre

We propose a new physics-based RTN/LFN variability model. We explain why variability of RTN/LFN doesn't follow a $1/\sqrt{\text{area}}$ dependency. The model validity is demonstrated through numerous results for n-channel and p-channel devices from different CMOS nodes. We show that the variability depends on bias, providing physical interpretations of these observations.

2:25 p.m.
35.3 Experiment and Model for Deviation from Pelgrom Scaling Relation in Device Width, N. Lu, J. Brown, R. Thoma, P. Kotecha and R. Wachnik, IBM Semiconductor Research and Development Center

We show that FETs exhibit several width dependent characteristics purely due to un-correlated random variations among sub-threshold currents in different width segments. They include per-unit-width median sub-threshold current and constant-current threshold voltage. The width scaling relation for threshold voltage mismatch is different from Pelgrom scaling for sufficiently large variation.

2:50 p.m.
35.4 A Comprehensive Platform for Thermal Studies in TSV-based 3D Integrated Circuits, P.M. Souaré, P. Coudrain, J.P. Colonna*, V. Fiori, A. Farcy, F. de Crécy*, A. Borbely**, H. Ben-Jamaa*, C. Laviron*, S. Gallois-Garreignot, B. Giraud*, N. Hotellier, R. Franiatte*, S. Dumas, C. Chancel*, J.M. Rivière, J. Pruvost, S. Chéramy*, C. Tavernier, J. Michailos and L. Le Pailleur, STMicroelectronics, *CEA-Leti, Minatec, Université Grenoble Alpes, **Ecole des Mines de Saint Etienne

We present an advanced and comprehensive platform for thermal dissipation studies in TSV-based 3D ICs. A 2-tier 3D test chip with through silicon via (TSV) and µ-bump is used for thermal characterization with unprecedented precision and design exploration capabilities. A comprehensive calibrated 3D finite element model is associated to provide a predictive tool that is able to simulate the thermal mapping in any given 3D interconnect configuration with minimal error. Guidelines are finally provided for thermal optimization of 3D designs with a precision far beyond the prior art.

3:15 p.m.
35.5 A New Surface Potential-Based Compact Model for a-IGZO TFTs in RFID Applications, Z. Zong, L. Li, J. Jang*, Z. Li, N. Lu, L. Shang, Z. Ji and M. Liu, Institute of Microelectronics of Chinese Academy of Sciences, *Kyung Hee University

For the first time, we present a surface potential-based compact model for a-IGZO TFTs based on multiple trapping-release theory and benchmark our work against device measurements. This model does not require time-consuming

calculation. Meanwhile, we have developed the automatic parameter extraction program, which can extract the parameters rapidly and accurately. Moreover, the compact model is coded in Verilog-A, and implemented in a vendor CAD environment. The model provides physics-based consistent description of DC and AC device characteristics and enables accurate circuit-level performance estimation and RFID circuit design of a-IGZO TFTs.

3:40 p.m.
35.6 Physics-Based Factorization of Magnetic Tunnel Junctions for Modeling and Circuit Simulation, K. Camsari, S. Ganguly, S. Datta and D. Datta*, Purdue University, *GLOBALFOUNDRIES

A simple yet powerful device model for Magnetic Tunnel Junction devices is presented. Proposed model "factorizes" Magnetic Tunnel Junctions into simpler building blocks that are described by experimentally and theoretically accessible material parameters. The model captures all voltage/angle dependent MTJ features and matches results of ab-initio theories' results analytically. The generality of the physics-based factorization approach is illustrated by demonstrating it can be used on Spin-Valves. Proposed model can be used as a predictive modeling tool for emerging MTJ devices, entirely within a SPICE/Verilog-A based framework due to its parametric simplicity.