Session 34: Characterization, Reliability, and Yield – Reliability: BTI, HCI and Breakdown
Wednesday, December 17, 1:30 p.m.
Continental Ballroom 7-9
Co-Chairs: Souvik Mahapatra, IIT Bombay
Ziyuan Liu, Renesas Electronics

1:35 p.m.
34.1 New Insights into the Design for End-of-life Variability of NBTI in Scaled High-k/Metal-gate Technology for the nano-Reliability Era, P. Ren, R. Wang, Z. Ji*, P. Hao, X. Jiang, S. Guo, M. Luo, M. Duan*, J. Zhang*, J. Wang**, J. Liu**, W. Bu**, J. Wu**, W. Wong**, S. Yu**, H. Wu**, S.-W. Lee**, N. Xu*** and R. Huang, Peking University, *Liverpool John Moores University, **Semiconductor Manufacturing International Corporation, ***University of California, Berkeley

In this paper, a new methodology for the assessment of end-of-life variability of NBTI is proposed for the first time. By introducing the concept of characteristic failure probability, the uncertainty in the predicted 10-year *VDD* is addressed. Based on this, variability resulted from NBTI degradation at end of life under specific *VDD* is extensively studied with a novel characterization technique. With the further circuit level analysis based on this new methodology, the timing margin can be relaxed. The new methodology has also been extended to FinFET in this work. The wide applicability of this methodology is helpful to future reliability/variability-aware circuit design in nano-CMOS technology.

2:00 p.m.
34.2 NBTI of Ge pMOSFETs: Understanding Defects and Enabling Lifetime Prediction, J. Ma, W. Zhang, J.F. Zhang, B. Benbakhti, Z. Ji, J. Mitard*, J. Franco*, B. Kaczer* and G. Groeseneken*, Liverpool John Moores University, *IMEC

Conventional lifetime prediction method developed for Si is inapplicable to Ge devices. This work demonstrates that the defects are different in Ge and Si devices. For the first time, a method is developed for Ge devices to restore the power law for NBTI kinetics, which assists in Ge process/device optimization.

2:25 p.m.
34.3 Accurate Prediction of PBTI Lifetime in N-type Fin-Channel High-k Tunnel FETs, W. Mizubayashi, T. Mori, K. Fukuda, Y.X. Liu, T. Matsukawa, Y. Ishikawa, J. Tsukada, H. Yamauchi, Y. Morita, S. Migita, H. Ota and M. Masahara, National Institute of Advanced Industrial Science and Technology (AIST)

The positive bias temperature instability (PBTI) characteristics for n-type fin-channel tunnel FETs (TFETs) with HK have been thoroughly investigated and compared with conventional FinFETs. The subthreshold slope (SS) is not degraded at all while the threshold voltage (V_{th}) shifts in the positive direction by the PBTI stress. The activation energy of ΔVth for the TFETs is almost the same as FinFETs, indicating that the PBTI mechanism for the TFETs is almost the same as FinFETs. It was found, by applying a positive bias to the n^+-drain (normal operation condition), the PBTI lifetime is dramatically improved as compared with that in conventional stress test (both p^+-source and n^+-drain are grounded). This is because the carrier injection from the n+-drain is the main cause of the PBTI especially for the n-type TFET. Thus, the realistic impact of PBTI is significantly mitigated for the n-type TFET.

2:50 p.m.
34.4 BTI Reliability of Advanced Gate Stacks for Beyond-Silicon Devices: Challenges and Opportunities (Invited), G. Groeseneken, J. Franco, M. Cho, B. Kaczer, M. Toledano-Luque, P. Roussel, T. Kauerauf, A. Alian, J. Mitard, H. Arimura, D. Lin, N. Waldron, S. Sioncke, L. Witters, H. Mertens, L.-Å Ragnarsson, M. Heyns, N. Collaert, A. Thean and A. Steegen, imec

When developing novel Beyond-Si high-mobility channel device technologies, next to the drive current and mobility, the BTI reliability is one of the important performance parameters that should be accounted for when deciding the optimal stack. In this paper we review our present understanding of BTI in Si and Beyond-Si based sub 1-nanometer EOT MOSFET devices. Based on the framework model we developed for SiGe stacks we benchmark alternative Beyond-Si gate stacks using a metric for carrier-defect decoupling, allowing to screen stacks for acceptable reliability.

3:15 p.m.

34.5 New Understanding of State-Loss in Complex RTN: Statistical Experimental Study, Trap Interaction Models, and Impact on Circuits, J. Zou, R. Wang, S. Guo, M. Luo, Z. Yu, X. Jiang, P. Ren, J. Wang, J. Liu, J. Wu, W. Wong, S. Yu, H. Wu, S.-W. Lee, Y. Wang and R. Huang, Peking University, *Semiconductor Manufacturing International Corporation

In this paper, the statistical characteristics of complex RTN (both DC and AC) are experimentally studied for the first time, rather than limited case-by-case studies. It is found that, over 50% of RTN-states predicted by conventional theory are lost in actual complex RTN statistics. Based on the mechanisms of non-negligible trap interactions, new models are proposed, which successfully interpret this state-loss behavior, as well as the different complex RTN characteristics in SiON and high-k devices. The circuit-level study also indicates that, predicting circuit stability would have large errors if not taking into account the trap interactions and RTN state-loss. The results are helpful for the robust circuit design against RTN.

3:40 p.m.
34.6 New Observations on Hot Carrier Induced Dynamic Variation in Nano-scaled SiON/Poly, HK/MG and FinFET Devices Based on On-the-fly HCI Technique: The Role of Single Trap Induced Degradation, C. Liu, K.T. Lee, S. Pae and J. Park, Samsung Electronics

In this paper, HCI induced dynamic variation in nano-scaled MOSFETs is systematically studied. Based on the proposed on-the-fly HCI technique, individual defect related HCI variation in small area device is observed for the first time. The fundamental properties of HCI variation sources (single trap induced degradation and trap number) are further investigated. The results show universal scaling trend for all the SiON/Poly, HK/MG and FinFET devices which confirms that the device dimension scaling is the main driving force for the enhanced individual trap effect. Based on the new observations, HCI variation model is further discussed for the accurate prediction for design. Moreover, HCI variation is compared with BTI and RTN in terms of individual trap. The results show that HCI effect has the largest single trap impacts, which implies the defects responsible for HCI could be mainly located near or at the dielectric-silicon interface.

4:05 p.m.
34.7 Multiple Breakdown Phenomena and Modeling for Non-Uniform Dielectric Systems, E. Wu, B. Li, J. Stathis and R. Achanta, IBM Co., SRDC

In this work, we present successive BD theory of time-dependent clustering model and its verification with several sets of experimental data using grouping methodology. To go beyond the use of grouping method, we will present a wide range of experimental observations of multiple BD phenomena involving clustering and bimodality effects with or without BD correlation for several dielectric systems. More importantly, we report the anti-correlation effects observed in BEOL TDDB. The understanding of these effects can lead to much improved understanding of breakdown statistics and much needed reliability margin for 10nm technology node and beyond.