Session 33: Nano Device Technology – Exploratory Devices
Wednesday, December 17, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: Bernard Dieny, CEA/SPINTEC
Elena Gnani, University of Bologna

1:35 p.m.
33.1 Experimental Demonstration of Four-Terminal Magnetic Logic Device with Separate Read- and Write-Paths, D. Bromberg, M. Moneck, V. Sokalski, L. Pileggi and J.-G. Zhu, Carnegie Mellon University

Magnetic logic has recently become an attractive candidate for future electronics. This paper describes the demonstration of a four-terminal spintronic device with distinct read- and write-paths and gain sufficient to drive fanout independent of CMOS. Measured data on test structures and prototype devices are presented.

2:00 p.m.
33.2 Perpendicular-anisotropy CoFeB-MgO Based Magnetic Tunnel Junctions Scaling Down to 1X nm, S. Ikeda, H. Sato, E.C.I. Enobio, S. Ishikawa, M. Yamanouchi, S. Fukami, F. Matsukura, T. Endoh and H. Ohno, Tohoku University

We investigate properties of perpendicular-anisotropy magnetic tunnel junctions (p-MTJs) with double-interface CoFeB-MgO recording layer at a reduced dimension down to 1X nm fabricated by hard-mask process. The ratio of thermal stability factor to intrinsic critical current increases with decreasing junction size.

2:25 p.m.
33.3 High Performance, Excellent Reliability Multifunctional Graphene Oxide Doped Memristor Achieved by Self-protective Compliance Current Structure, K.-C. Chang, R. Zhang, T.-C. Chang, T.-M. Tsai, T.-J. Chu, H.-L. Chen, C.-C. Shih, S.-Y. Huang, C.-H. Pan and M. Sze, National Sun Yat-Sen University, *Peking University, **Stanford University

Two-sided graphene oxide doped silicon oxide based RRAM with filament self-aligning formation, self-current limiting operation, CRS application, whole cycle multi-bit ability is demonstrated. The device exhibits outstanding performance including switching speed (~30ns) at low operation voltage, endurance property (> one Tera-cycles), read disturbance immunity (>ten Giga-cycles), retention (> ten kilo-second at 125℃).

2:50 p.m.
33.4 Realizing a Topological-Insulator Field-effect Transistor using Iodostannanane, W. Vandenberghe and M. Fischetti, University of Texas at Dallas

We calculate the conductivity and mobility of monolayer tin functionalized with iodine and show that its topological insulating nature leads to a strong dependence of the conductivity on the Fermi level. We show how this property can be exploited to build a new kind of transistor: the topological-insulator field-effect transistor.

3:15 p.m.
33.5 Hybrid Si/2D Electronic Double Channels Fabricated Using Solid Few-Layer-MoS_2 Stacking for V_{th} Matching and CMOS-Compatible 3DFETs, M.-C. Chen, C.-Y. Lin, K.-H. Li, L.-J. Li, C.-H. Chen, C.-H. Chuang, M.-D. Lee, Y.-J. Chen, Y.-F. Hou, C.-H. Lin, C.-C. Chen, B.-W. Wu, C.-S. Wu, I. Yang, Y.-J. Lee, W.-K. Yeh, T. Wang and F.-L. Yang, National Nano Device Laboratories, *Academia Sinica, **Tamkang University, ***National Chiao-Tung University

Stackable MoS_2 3DFETs containing hybrid Si/2D electronic double channels were developed by using a fully CMOS-compatible process. Several molecular layers (3–16 X) of transition-metal dichalcogenide material, MoS_2, exhibited an improved (25%) $I_{on,n}$ in the hybrid Si/2D electronic double channels 3DFETs. The PFETs operated effectively and the N/PMOS V_{th} matched perfectly. The proposed heterogeneous hybrid Si/2D electronic double channels 3DFETs can enhance scaled device performance in applications that require technology more advanced than 7 nm CMOS technology.

3:40 p.m.

33.6 High-Performance Carbon Nanotube Transistors, M. Shulaker, G. Pitner, G. Hills, M. Giachino, H.-S. P. Wong and S. Mitra, Stanford University

Carbon nanotube-based digital electronics promise both increased performance and improved energy efficiency beyond the limitations of current silicon-based transistors. Low carbon nanotube density is a major obstacle that must be overcome to achieve the high current drive (I_{on}) necessary for high-performance and highly energy-efficient carbon nanotube digital logic circuits. We reproducibly demonstrate carbon nanotube field-effect transistors (CNFETs) with the highest current drive (per unit layout width) to-date, (>100 μA/μm at 400 nm channel length) while simultaneously achieving high I_{on}/I_{off} (>5000). This is the first demonstration of CNFETs with nominal density above 100 CNTs/μm with highly aligned CNTs, with current drives approaching that of similarly-scaled, similarly-biased silicon-based field-effect transistors in production in major semiconductor foundries.