**Session 32: Process and Manufacturing Technology – Advanced Process Modules**
Wednesday, December 17, 1:30 p.m.
Grand Ballroom A
*Co-Chairs:* Muhsin Celik, STMicroelectronics
Chorng-Ping Chang, AMAT

1:35 p.m.
**32.1 Electrical Characterization of FinFET with Fins Formed by Directed Self Assembly at 29 nm Fin Pitch Using a Self-Aligned Fin Customization Scheme,** H. Tsai, H. Miyazoe, J. Chang, J. Pitera, C.-C. Liu, M. Brink, I. Lauer, J. Cheng, S. Engelmann, J. Rozen, J. Bucchignano, D. Klaus, S. Dawes, L. Gignac, C. Breslin, E. Joseph, D. Sanders, M. Colburn and M. Guillorn, IBM Watson Research Center, IBM Albany Nanotech Research Center, IBM Research Almaden,

We demonstrated a fin circuit patterning technique with self-aligned fin customization using 29nm-pitch PS-PMMA directed self-assembly (DSA). Electrical data produced from fins patterned with this approach shows good uniformity and no signs of gross CD variation. Proper design of the DSA templates improved process uniformity and lowered defectivity.

2:00 p.m.
**32.2 Highly Reliable Cu Interconnect Strategy for 10nm Node Logic Technology and Beyond,** R.-H. Kim, B.H. Kim, T. Matsuda, J.N. Kim, J.M. Baek, J.J. Lee, J.O. Cha, J.H. Hwang, K.H. Park, J.K. Choi, D.H. Lee, I.S. Kim, E.B. Lee, S.D. Nam, Y.W. Cho, D.W. Park, H.J. Choi, J.S. Kim, S.Y. Jung, S.H. Park, H.B. Lee, S.H. Ahn, B.U. Yoon, S.S. Paak, N.-I. Lee, J.-H. Ku, J.S. Yoon, H.-K. Kang and E.S. Jung, Samsung Electronics Co., Ltd.

CVD-Ru liner / Reflow-Cu scheme is adopted for 10nm node BEOL technology, demonstrating superior gap-fill performance and robust reliability. Pattern dependence of reflow Cu scheme is tightly controlled based on the suggested failure modeling. Furthermore, integration and reliability challenges at 10nm node technology, associated with Ru liner, are identified and addressed. Successful multi-level integration with optimized CMP process suggests CVD Ru liner as an appealing candidate for 10nm node technology and beyond.

2:25 p.m.
**32.3 A New High-k/metal Gate CMOS Integration Scheme (Diffusion and Gate Replacement) Suppressing Gate Height Asymmetry and Compatible with High-thermal Budget Memory Technologies,** R. Ritzenthaler, T. Schram, A. Spessot*, C. Caillat*, M. Cho, E. Simoen, M. Aoulaiche, J. Albert, S.A. Chew, K.B. Noh**, Y. Son**, P. Fazan*, N. Horiguchi and A. Thean, imec, *Micron, **SK-Hynix

In this work, a new scheme (Diffusion and gate replacement (D&GR)) for MIPS integration is demonstrated. The CMOS flow allows to control the gate height asymmetry between N and P stacks, driving the work function shifter in the high-k. Since the dopants source is removed, it improves the integration friendliness for high-thermal budget processes, such as control logic for memory technologies, making it an optimal choice for DRAM periphery.

2:50 p.m.
**32.4 Ultra Low Contact Resistivity (< $1x10^{-8}$ Ω- cm$^2$) to $In_{0.53}Ga_{0.47}As$ Fin Sidewall (110)/(100) Surfaces: Realized with a VLSI Processed III-V Fin TLM Structure Fabricated on III-V on Si Substrates,** R.T.P. Lee, Y. Ohsawa*, C. Huffman, Y. Trickett*, G. Nakamura*, C. Hatem**, K.V. Rao**, F. Khaja**, R. Lin***, K. Matthews, K. Dunn^, A. Jensen***, T. Karpowicz***, P. Nielsen***, E. Stinzianni, A. Cordes, P.Y. Hung, D.-H. Kim^, R.J.W. Hill, W.-Y. Loh and C. Hobbs, SEMATECH, *Tokyo Electron Technology Center, **Applied Materials, ***CAPRES A/S, ^College of Nanoscale Science and Engineering, ^^GLOBALFOUNDRIES

We report a record low contact resistivity of sub-$1.0x10^{-8}$ Ω. cm$^2$ realized on n+ $In_{0.53}Ga_{0.47}As$ fin sidewall surfaces. This is achieved with VLSI processed fin TLM structures on wafer scale III-V on Si substrates. A novel low-damage III-V fin etch was developed and fins down to 35 nm were fabricated. A surface treatment to smoothen the fin sidewall surfaces was proposed, which reduced sidewall surface roughness variation by 90%. Additionally, we show for the first time that implant temperature could be used to eliminate implant damage in III-V fins. This increased activation efficiency (+3.6x) and reduced sheet resistance (-60%).

3:15 p.m.

**32.5 Dramatic Effects of Hydrogen-induced Out-diffusion of Oxygen from Ge Surface on Junction Leakage as well as Electron Mobility in n-channel Ge MOSFETs,** C.H. Lee, T. Nishimura, C. Lu, S. Kabuyanagi and A. Toriumi, The University of Tokyo

This paper discusses about oxygen effects on Ge substrate from both viewpoints of advantages and disadvantages in MOSFET performance. For improvement of electron mobility in Ge n-FETs, oxygen in the channel region should be extracted to prevent additional scattering. On the other hand, oxygen in S/D region is helpful for dramatically suppressing junction leakage currents. By understanding these oxygen effects on Ge, high electron mobility Ge n-FETs with highest Ion/Ioff ratio is demonstrated.

3:40 p.m.
**32.6 Evolution of Directed Ion Beams from Doping to Materials Engineering,** A. Renau, Applied Materials, VSE

We review recent changes to implanter processing capabilities, including the adoption of cryogenic implants to reduce leakage and contact resistance and high temeperature implants for finFETs. We discusss some specific 3D challenges and introduce a new process technology for 3D that uses directed ion beams in a plasma chamber.

4:05 p.m.
**32.7 A Novel Junctionless FinFET Structure with Sub-5nm Shell Doping Profile by Molecular Monolayer Doping and Microwave Annealing,** Y.-J. Lee, T.-C. Cho*, K.-H. Kao**, P.-J. Sung, P.-C. Huang*, F.-K. Hsueh, C.-T. Wu, S.-H. Hsu, W.-H. Huang, Y. Li*, M.I. Current***, B. Hengstebeck^, J. Marino^, J.-M. Shieh, T.-S. Chao* and W.-K. Yeh, National Nano Device Laboratories, *National Chiao Tung University, **National Cheng Kung University, ***Current Scientific, ^Evans Analytical Group

For the first time, a novel junctionless (JL) FinFET structure with a shell doping profile (SDP) formed by molecular monolayer doping (MLD) method and microwave annealing (MWA) at low temperature is proposed and studied. Thanks to a better gate control, a JLFinFET with the SDP can retain the ideal subthreshold swing (~60 mV/dec) at a high doping level. Poly-Si n & p JLFinFETs (W/L=10/20 nm) with SDP experimentally exhibit superior gate control ($I_{on}/I_{off} > 10^6$)and improved device variation.