Session 30: Modeling and Simulation – Novel Materials and Devices for FETs
Wednesday, December 17, 9:00 a.m.
Imperial Ballroom A
Co-Chairs: Liang Gengchiau, National University of Singapore
Suman Banerjee, Texas Instruments

9:05 a.m.
30.1 Source-induced RDF Overwhelms RTN in Nanowire Transistor: Statistical Analysis with Full Device EMC/MD Simulation Accelerated by GPU Computing, A. Suzuki, T. Kamioka, Y. Kamakura, K. Ohmori, K. Yamada and T. Watanabe, Waseda University, *Toyota Technological Institute, **Osaka University, ***University of Tsukuba

We demonstrate numerically that the random dopant fluctuation (RDF) in source region causes a noticeable variability in the on-current of Si nanowire (NW) transistors, and its impact is found to be much larger than that of random telegraph noise (RTN). This work assesses static and dynamic variability of NW device characteristics by means of the Ensemble Monte Carlo / Molecular dynamics (EMC/MD) simulation, making use of the parallel computing technique with graphic processing unit (GPU). The current flow in one-dimensional NW device is almost decided by the number of dopants at the source edge, indicating the importance of forming abrupt source-channel boundary to suppress the variability.

9:30 a.m.
30.2 Perspective of Tunnel-FET for Future Low-power Technology Nodes, A. Verhulst, D. Verreck, Q. Smets, K.-H. Kao, M. Van de Put, R. Rooyackers, B. Sorée, A. Vandooren, K. De Meyer, G. Groeseneken, M. Heyns, A. Mocuta, N. Collaert and A. V.-Y. Thean, imec

This paper starts with a calibration of the band-to-band tunneling (BTBT) models. It then discusses architecture and material optimizations, highlights the differences between n-TFET and p-TFET, and focuses on unexplored material aspects, like decrease of dielectric constant with confinement. Parasitic effects are briefly touched upon, with trap-assisted tunneling (TAT) being the most challenging TFET parasitic to overcome. A new metric, VTAT, is defined to capture the TAT impact.

9:55 a.m.
30.3 Performance Evaluation of MoS_2-WTe_2 Vertical Tunneling Transistor using Real-space Quantum Simulator, K.-T. Lam, G. Seol and J. Guo, University of Florida

Interlayer transport through a MoS_2-WTe_2 PN heterojunction is studied by atomistic quantum simulation based on non-equilibrium Green's function formalism in the ballistic limits. Ultra-steep subthreshold slope and low leakage current are observed, which are found to be robust against dominant extrinsic scattering mechanism such as atomic defects and charged impurity.

10:20 a.m.
30.4 *Ab-initio* Simulations of MoS_2 Transistors: from Mobility Calculation to Device Performance Evaluation, A. Szabo, R. Rhyner and M. Luisier, ETH Zurich

We present the first ab-initio quantum transport simulations of metal dichalcogenide transistors taking electron-phonon scattering into account. We will demonstrate that the phonon-limited electron mobility of MoS2 reaches values up to 220 cm^2/Vs and drops at high carrier concentrations and that MoS_2 cannot compete with strained Si or III-V as next-generation high performance switch.

10:45 a.m.
30.5 Performance Evaluation and Design Considerations of 2D Semiconductor Based FETs for Sub-10 nm VLSI, W. Cao, J. Kang, D. Sarkar, W. Liu and K. Banerjee, University of California, Santa Barbara

Two-dimensional (2D) semiconductors, such as the well-known molybdenum disulfide (MoS_2), are witnessing an explosion in research activities due to their apparent potential for sub-10-nm node very-large-scale-integration (VLSI) applications. In this paper, dissipative quantum transport simulations using non-equilibrium Green's function (NEGF) formalism are performed to rigorously evaluate the scalability and performance of monolayer/multilayer 2D semiconductor based FETs with MoS_2 as an example channel material. Device design considerations in terms of the choice of prospective 2D material/structure/technology to fulfill sub-10-nm ITRS requirements are analyzed for the first

time. Firstly, it is found that MoS_2 FETs can meet high-performance (HP) requirement up to 6.6 nm by using bilayer MoS_2 as the channel material, while low-standby-power (LSTP) requirements present significant challenges for all sub-10 nm nodes. Secondly, by studying the effects of underlap (UL) structures, scattering strength and carrier effective mass, it is found that the high mobility and suitably low effective mass of tungsten diselenide (WSe2), aided by UL, enable 2D FETs for both HP and LSTP applications at the smallest foreseeable (5.9 nm) node. Finally, possible solutions for sub-5 nm nodes are also proposed based on the effects of critical parameters on device performance.

11:10 a.m.

30.6 Atomic Disorder Scattering in Emerging Transistors by Parameter-Free First Principle Modeling, Q. Shi, L. Zhang*, Y. Zhu**, L. Liu**, M. Chan* and H. Guo, McGill University, *Hong Kong University of Science and Technology, **NanoAcademic Technologies Inc.

For the first time we report a parameter-free first principle modeling methodology for atomic disorder effects in realistic transistors. Based on the NECPA theory for disorder scattering and a sparse Hamiltonian implementation, it has a linear scalability in computational intensity. These merits are demonstrated with a (B-N) co-doped graphene TFET.