

## Session 29: Memory Technology – PCM and Neural Networks

Wednesday, December 17, 9:00 a.m.

Continental Ballroom 6

*Co-Chairs:* Paola Zuliani, STMicroelectronics  
Guisseppina Puzzilli, Micron

9:05 a.m.

**29.1 Optimization Metrics for Phase Change Memory (PCM) Cell Architectures**, M. Boniardi, A. Redaelli, C. Cupeta, F. Pellizzer, L. Crespi\*, G. D'Arrigo\*\*, A. Lacaíta\* and G. Servalli, Micron Semiconductor Italia s.r.l., \*Politecnico di Milano, \*\*Consiglio Nazionale delle Ricerche - Istituto per la Microelettronica e Microsistemi (CNR-IMM)

Different Phase-Change Memory (PCM) cell architectures, based on  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST) active material, have been fabricated and analyzed in terms of program and read efficiency and integration. Despite self-heating approaches have better efficiency, the Wall architecture is shown to be the easiest for process integration, still matching electrical target. Further optimization of the wall architecture, based on a simple model, is then discussed.

9:30 a.m.

**29.2 55- $\mu\text{A}$   $\text{Ge}_x\text{Te}_{1-x}/\text{Sb}_2\text{Te}_3$  Superlattice Topological-switching Random-access Memory (TRAM) and Study of Atomic Arrangement in Ge-Te and Sb-Te Structures**, N. Takaura, T. Ohyanagi, M. Tai, M. Kinoshita, K. Akita, T. Morikawa, H. Shirakawa\*, M. Araidai\*\*, K. Shiraishi\*\*, Y. Saito\*\*\* and J. Tominaga\*\*\*, Low-power Electronics Association Project, \*University of Tsukuba, \*\*Nagoya University, \*\*\*National Institute of Advanced Industrial Science and Technology

A  $\text{Ge}_x\text{Te}_{1-x}/\text{Sb}_2\text{Te}_3$  superlattice topological-switching random-access memory (TRAM) was developed. Set and reset currents of 55  $\mu\text{A}$ , the lowest for an ULSI-grade device, were obtained. TEM analyses of Ge-Te structures and novel superlattice fabrication enabled us to reveal the retention, endurance, and electrical characteristics of TRAM for the first time.

9:55 a.m.

**29.3 Phase Change Memory and its Intended Applications (Invited)**, C. Lam, IBM Research, T.J. Watson Research Center

Phase Change Memory (PCM) has been one of the emerging memories for more than a decade. Fundamentals of PCM have been studied in great detail, challenges have been identified, and device structures have been proposed and demonstrated. With this large body of knowledge, it is time to examine probable applications for PCM.

10:20 a.m.

**29.4 Capacity Optimization of Emerging Memory Systems: A Shannon-Inspired Approach to Device Characterization**, J.H. Engel, S.B. Eryilmaz\*, S. Kim\*\*, M. BrightSky\*\*, C. Lam\*\*, B.A. Olshausen and H.-S.P. Wong\*, University of California, Berkeley, \*Stanford University, \*\*IBM Research, T.J. Watson Research Center

We present a statistical framework for the characterization of analog-valued memory devices that enables co-optimization of device properties and memory controller design. Traditionally, the capacity (bits/device) is measured as the number of distinct states at a given Raw Bit Error Rate (RBER). Using Phase Change Memory (PCM) arrays, we demonstrate that measuring the mutual information allows optimal design of read-write circuits to increase capacity by 30%. We further show that this approach enables energy efficient memory design by optimizing simulations of a 1Mb memory array to consume 32% less energy/bit. This work provides an information-theoretic framework to guide the design and characterization of other analog-valued emerging memories such as RRAM and CBRAM.

10:45 a.m.

**29.5 Experimental Demonstration and Tolerancing of a Large-scale Neural Network (165,000 synapses), using Phase-change Memory as the Synaptic Weight Element**, G. Burr, R. Shelby, C. di Nolfo, J. Jang, R. Shenoy, P. Narayanan, K. Virwani, E. Giacometti, B. Kurdi and H. Hwang, IBM Almaden Research Center, \*Pohang University of Science and Technology

Using 2 phase-change memory (PCM) devices per synapse, a 3-layer perceptron network with 164,885 synapses is trained on a subset (5000 examples) of the MNIST database of handwritten digits using a backpropagation variant suitable for NVM+selector crossbar arrays, obtaining a training (generalization) accuracy of 82.2% (82.9%). Using a neural network (NN) simulator matched to the experimental demonstrator, extensive tolerancing is performed with respect to NVM variability, yield, and the stochasticity, linearity and asymmetry of NVM-conductance response.

11:10 a.m.

**29.6 Statistics of Set Transition in Phase Change Memory (PCM) Arrays**, M. Rizzi, N. Ciocchini, S. Caravati\*, M. Bernasconi\*, P. Fantini\*\* and D. Ielmini, Politecnico di Milano and IU.NET, \*Università degli Studi di Milano-Bicocca, \*\*Micron Technology Inc.

This work addresses set transition in PCM arrays, providing evidence for a thickness-dependent set time and of its statistical spread. We compare the set-transition energy with 2 different methods, namely square and triangular pulse, providing guiding rules for minimizing the energy consumption and switching variability in PCM.

11:35 a.m.

**29.7 Circuit-Level Benchmarking of Access Devices for Resistive Nonvolatile Memory Arrays**, P. Narayanan, G. Burr, R. Shenoy, K. Virwani and B. Kurdi, IBM Research - Almaden

Access Devices (1AD) for crossbar resistive (1R) memories are compared via circuit-level analysis. We show that in addition to intrinsic properties, AD suitability for 1AD1R memories is strongly dependent upon (a) nonvolatile memory (NVM) and (b) circuit parameters. We find that (1) building large arrays ( $\geq 1\text{Mb}$ ) with  $\geq 10\mu\text{A}$  NVM current would require MIEC ADs and moderate NVM switching voltage ( $\leq 1.2\text{V}$ ). (2) For all ADs high NVM voltages ( $> 2\text{V}$ ) are supported only at sub- $5\mu\text{A}$  currents. AD improvements to expand this design space are discussed.

12:00 p.m.

**29.8 A Novel Inspection and Annealing Procedure to Rejuvenate Phase Change Memory from Cycling-Induced Degradations for Storage Class Memory Applications**, W.S. Khwa, J.Y. Wu, T.H. Su, H.P. Li, M. BrightSky\*, T.Y. Wang, T.H. Hsu, P.Y. Du, S. Kim\*, W.C. Chien, R. Cheek\*, E.K. Lai, Y. Zhu\*, M.H. Lee, M.F. Chang\*\*, H.L. Lung and C. Lam\*, Macronix International Co., Ltd., \*IBM T.J. Watson Research Center, \*\*National Tsing Hua University

A novel Cycle Alarm Point (CAP) inspection is proposed to monitor PCM cycling degradation. We further propose an In-Situ-Self-Anneal (ISSA) procedure, such that once a CAP is detected, the annealing procedure is issued to rejuvenate the cells. We demonstrate, for the first time, PCM cycling degradation can be recovered repeatedly.