**Session 27: Process and Manufacturing Technology – Hybrid and 3D Integration**
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 4
*Co-Chairs:* Maud Vinet, CEA-LETI
Carlos Mazure, SOITEC

9:05 a.m.
**27.1 Wafer Level System Integration for SiP,** D.C.H. Yu, Taiwan Semiconductor Manufacturing Company

A family of novel wafer-level-system-integration technologies (WLSI) was proposed. This paper reviews WLSI feasibility work first. Further results on the reliability, the compatibility of the integration with both more advanced node Logic and DRAM devices, and the higher-level system integration of the WLSI technologies are then presented. Foundry has established a comprehensive system integration technology portfolio in wafer form to fulfill the needs from mobile to cloud computing for the future growth of the Si-based nano-electronics industry.

9:30 a.m.
**27.2 High-precision Wafer-level Cu-Cu Bonding for 3DICs,** M. Okada, I. Sugaya, H. Mitsuishi, H. Maeda, T. Shimoda, S. Izumi, H. Nakahira and K. Okamoto, Nikon Corporation

We report a high-precision Cu-Cu bonding system for 3DICs fabrication adopting a new precision alignment methodology and a new pressure profile control system. Experimental results show that the alignment capability is 250 nm or better, and the overlay accuracy of the permanent bonded wafers is 260 nm ($|\text{average}| + 3\sigma$).

9:55 a.m.
**27.3 A Manufacturable Interposer MIM Decoupling Capacitor with Robust Thin high-K Dielectric for Heterogeneous 3D IC CoWoS System Integration,** W.-S. Liao, C.H. Chang, S.W. Huang, T.H. Liu, H.P. Hu, H.L. Lin, C.Y. Tsai, C.S. Tsai, H.C. Chu, C.Y. Pai, W.C. Chiang, S.Y. Hou, S.P. Jeng and D. Yu, Taiwan Semiconductor Manufacturing Company

A reliability proven high-K (HK) metal-insulator-metal (MiM) structure has been verified within the silicon interposer in a chip-on-wafer-on-substrate (CoWoS) packaging for heterogeneous system-level decoupling application. The HK dielectric has an equivalent oxide thickness (EOT) of 20Å, intrinsic TDDB lifetime of 322 years at an operation voltage ($V_{cc}$) of 1.8V, and a leakage current ($I_{LK}$) well below 1 fA/μm$^2$ under 2V at 125°C. The measured unit area capacitance density for the single, 2- and 3-in-series HK MiM combination is 17.2, 4.3 and 1.9 fF/μm$^2$, respectively, with their corresponding $I_{LK}$ below 0.48, 0.19 and 0.09 fAmp/μm2. Process reliability related defect density ($D_0$) of the MiM is as low as 0.095% cm$^{-2}$ as judged by a 10 year lifetime breakdown voltage ($V_{bd}$) criterion of 3.2V. This low D0 ensures the MiM to be used in a large area over 1056 cm$^2$ within the Si interposer. Moreover, the Vbd tolerance of the MiM can be drastically enhanced to be 9.75 and 14.25V, respectively, by 2- and 3-in series connection. At the package level during all steps of CoWoS processing, no distinguishable process induced damage (PID) and performance degradation (Cap., $I_{LK}$ & $V_{bd}$ tailing) were detected. Therefore, this high capacitance, low leakage, large area and reliability-proven interposer decoupling capacitor (DeCAP) within CoWoS greatly enhances the merit of using Si interposer for multi-chip system-level integration.

10:20 a.m.
**27.4 Monolithic 3D Integration of Logic and Memory: Carbon Nanotube FETs, Resistive RAM, and Silicon FETs,** M. Shulaker, T. Wu, A. Pal, K. Saraswat, H.-S.P. Wong and S. Mitra, Stanford University

We demonstrate, for the first time, monolithic 3D integration of logic and memory in arbitrary stacking order, with the ability to connect between any circuit layers. We experimentally show 4 vertically-stacked circuit layers (logic layer followed by two memory layers followed by a logic layer), enabled by integrating traditional silicon-FETs with low processing temperature emerging nanotechnologies: resistive random-access memory (RRAM), and carbon nanotube-FETs (CNFETs). This integration results in a robust monolithic 3D technology: memory and logic performance is invariant to the layer fabrication order. As a demonstration, we show a routing element of a switchbox for an FPGA, with each logic and memory element split between the 4 vertical layers.

10:45 a.m.

**27.5 New Insights on Bottom Layer Thermal Stability and Laser Annealing Promises for High Performance 3D Monolithic Integration,** C. Fenouillet-Beranger, B. Mathieu, B. Previtali, M.-P. Samson*, N. Rambal, V. Benevent, S. Kerdiles, J.-P. Barnes, J.-M. Hartmann, P. Besson, R. Kachtouli, P. Batude, F. Nemouchi, K. Huet**, I. Toqué-Trésonne**, D. Lafond, H. Dansas, F. Aussenac, G. Druais*, P. Perreau, E. Richard*, S. Chhun*, E. Petitprez*, N. Guillot*, F. Deprat, L. Pasini*, L. Brunet, V. Lu*, C. Reita and M. Vinet, CEA-LETI, *STMicroelectronics, **LASSE

For the first time the maximum thermal budget of in-situ doped source/drain State Of The Art (SOTA) FDSOI bottom MOSFET transistors is quantified to ensure transistors stability in Monolithic 3D (M3D) integration. Thanks to silicide stability improvement, the top MOSFET temperature could be relaxed up to 500°C. Laser anneal is then considered as a promising candidate for junctions activation. Thanks to in-depth morphological and electrical characterizations it shows very promising results for high performance Monolithic 3D integration.

11:10 a.m.

**27.6 Flexible High-performance Nonvolatile Memory by Transferring GAA Silicon Nanowire SONOS onto a Plastic Substrate,** J.-M. Choi, J.-W. Han* and Y.-K. Choi, KAIST, *NASA

Flexible nonvolatile memory is demonstrated with excellent memory properties comparable to the traditional wafer-based rigid type of memory. This achievement is realized through the transfer of an ultrathin film consisting of single crystalline silicon nanowire (SiNW) gate-all-around (GAA) SONOS memory devices onto a plastic substrate from a host silicon wafer.