Session 26: Display and Imaging Systems – Thin Film Transistors for Display and Large Area Electronic Applications
Wednesday, December 17, 9:00 a.m.
Continental Ballroom 1-3
Co-Chairs: David Gundlach, NIST
Francois Roy, STMicroelectronics

9:05 a.m.
26.1 Ultralow Power Transponder in Thin Film Circuit Technology on Foil with sub - 1V Operation Voltage, T.-H. Ke, K. Myny, A. Chasin*, R. Műller, P. Heremans* and S. Steudel, imec, *Ku Leuven

We demonstrate an organic complementary 8 bit transponder chip (XPDR) with Vdd down to 0.55V. Ultralow power consumption of 2.5 µW of the XPDR is realized. The XPDR can be powered by commercial AAA battery with ideal run-time of more than 100 years. The ultralow power thin film circuits on foil will open up new opportunities in ubiquitous sensing applications such as body area network and environmental monitoring wireless sensor networks.

9:30 a.m.
26.2 Thin-Film Heterojunction Field-Effect Transistors for Ultimate Voltage Scaling and Low-Temperature Large-Area Fabrication of Active-Matrix Backplanes, B. Hekmatshoar and A. Afzali-Ardakani, IBM T. J. Watson Research Center

Heterojunction field-effect thin-film transistors with crystalline Si channels and gate regions comprised of hydrogenated amorphous silicon or organic materials are demonstrated. The HJFET devices are processed at 200ºC and room-temperature, respectively; and exhibit operation voltages below 1V, subthreshold slopes of 70-100mV/dec and off-currents as low as 25 fA/um.

9:55 a.m.
26.3 High Performance Metal Oxide TFT and its Applications for Thin Film Electronics, G. Yu, C.-L. Shieh, J. Musolf, F. Foong, T. Xiao, G. Wang, K. Ottosson, CBRITE Inc.

Recent progress on metal-oxide TFT with mobility and stability as good as LTPS-TFT and with uniformity and off current as good as pristine a-Si TFT will be presented. Their applications for high pixel density displays and image arrays are discussed with emphasis on pixel and peripheral circuits with analog functions.

10:20 a.m.
26.4 Integration of Solution-Processed (7,5) SWCNTs with Sputtered and Spray-Coated Metal Oxides for Flexible Complementary Inverters, L. Petti, F. Bottacchi*, N. Münzenrieder, H. Faber*, G. Cantarella, C. Vogt, L. Büthe, I. Namal**, F. Späth**, T. Hertel**, T. D. Anthopoulos* and G. Tröster, Swiss Federal Institute of Technology, *Imperial College London, **University of Würzburg

We report the integration of solution-based p-type (7,5) SWCNTs with n-type metal oxides for the fabrication of high-performance complementary inverters. Flexible inverters based on SWCNTs and sputtered IGZO exhibit gains of 85 V/V while bent to 1 cm radius. We also realize flexible inverters based on SWCNTs and spray-coated InO_x.

10:45 a.m.
26.5 Solution-processed Poly-Si TFTs Fabricated at a Maximum Temperature of 150ºC, M. Trifunovic, J. Zhang, M. van der Zwan and R. Ishihara, Delft University of Technology

Poly-Si TFTs using liquid silicon are fabricated at a maximum processing temperature of 150°C by directly transforming polymerized cyclopentasilane to poly-Si using an Excimer Laser irradiation step, allowing solution processed Si TFT fabrication on substrates with a low cost and low thermal budget such as PET, PEN, and even paper.

11:10 a.m.
26.6 High Performance Ultra-Thin Body (2.4nm) Poly-Si Junctionless Thin Film Transistors with a Trench Structure, M.-S. Yeh, Y.-C. Wu, M.-H. Wu, Y.-R. Jhan, M.-H. Chung, Y.-C. Cheng and C.-C. Chung, National Tsing Hua University

The novel trench junctionless poly-Si thin-film transistor (trench JL-TFT) with ultra-thin body (2.4 nm) is utilized to simple dry etching process. The trench structure was successfully and easily integrated into the JL-TFT device. Additionally, the novel trench JL-TFT with NWs has show excellent performance in terms of low I_{OFF}, steep subthreshold swing (SS) of 99 mV/dec., no noticeable difference in the drain-induced barrier lowering (DIBL) value of 0 mV/V and high I_{ON}/I_{OFF} ratio of 10^7 A/A. Moreover, the trench JL-TFT can further increase the device I_{ON}/I_{OFF} ratio, and SS. The I_{ON} current of the UTB JL-TFT increases by quantum confined effect. Importantly, owing to its excellent device characteristics and simple fabrication, the trench JL-TFT is highly promising for use in advanced AMLCD, AMOLED and three-dimensional (3-D) stacked ICs applications.

11:35 a.m.

26.7 Performance Enhancement of a Novel P-type Junctionless Transistor Using a Hybrid Poly-Si Fin Channel for 3D IC Applications, Y.-C. Cheng, Y.-C. Wu, H.-B. Chen, J.-J. Su, C.-S. Shao, M.-S. Yeh and C.-Y. Chang, National Tsing Hua University, National Chiao Tung University

The hybrid fin poly-Si channel junctionless field-effect transistors (FET) are fabricated first. This novel devices show stable temperature/reliability characteristics, and excellent electrical performances in terms of steep SS (64mV/dec), high I_{on}/I_{off} ($>10^7$) and small DIBL (3mV/V). The devices are highly promising for future further scaling and 3D stacked ICs applications.