Session 25: Power and Compound Semiconductor Devices – III-V for Logic
Wednesday, December 17, 9:00 a.m.
Grand Ballroom A
Co-Chairs: Niamh Waldon, imec
Gilbert Dewey, Intel Corporation

9:05 a.m.
25.1 Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts, J. Lin, D. A. Antoniadis and J. A. del Alamo, Massachusetts Institute of Technology

We have fabricated self-aligned tight-pitch InGaAs Quantum-Well MOSFETs (QW-MOSFET) with scaled body thickness (tb) and metal contact length (Lc) by a novel fabrication process that features precise dimensional control. Impact of tb scaling on transport, resistance and short channel effects (SCE) have been studied. Thick tb is favorable for transport, and a mobility above 8000 cm^2/Vs is obtained. On the contrary, thin tb is beneficial for SCE control. A record gm,max of 3.1 mS/μm and R_{on} of 190 Ω-μm are obtained for L_g=80 nm. For the first time, working front-end device structures with contact size of 40 nm and gate-to-gate pitch size of 150 nm are demonstrated. They allow us to study the properties of nanoscale contacts. We derive a Mo to n^+ InGaAs cap contact resistivity of ro=$(8\pm2)\times10^{-9}$ $\Omega.cm^2$. This work presents new process technology and new insights on device physics that promise III-V MOSFET for high performance applications.

9:30 a.m.
25.2 High-Performance III-V Devices for Future Logic Applications (Invited), D.-H. Kim, J. A. del Alamo, D. A. Antoniadis, M. Urteaga*, B. Brar*, T.-W. Kim**, RH. Baek**, P. D. Kirsch**, W. Maszara***, H.-M. Kwon^, C.-S. Shin^^, W.-K. Park^^, YD Cho#, S.C. Shin#, D.H. Ko#, K.-S. Seo, MIT, *Teledyne Scientific Co., **SEMATECH, GLOBALFOUNDRIES, ***KANC, ^Yonsei University, ^^Seoul National University,

Indium-rich $In_XGa_{1-X}As$ (x>0.53) has recently emerged as the most promising non-Si n-channel material for post Si CMOS logic applications [1]. This is thanks to its outstanding electron transport characteristics and the excellent progress in the area of InGaAs MOSFETs, such as good interfacial quality of the high-k/InGaAs MOS by ALD and co-integration with Si. This paper reviews high-performance III-V devices for future logic applications, covers recent advances in some of the key enabling technology of InGaAs MOSFETs, and finally discusses options to further improve the performance of InGaAs MOSFETs.

9:55 a.m.
25.3 CMOS Compatible Self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs with GMSAT over 2200 μS/μm at V_{DD} = 0.5 V, Y. Sun, A. Majumdar, C. Cheng, R. Martin, R. Bruce, J. Yau, D. Farmer, Y. Zhu, M. Hopstaken, M. Frank, T. Ando, K. Lee, J. Rozen, A. Basu, K. Shiu, P. Kerber, D. Park, V. Narayanan, R. Mo, D. Sadana and E. Leobandung, IBM T.J. Watson Research Center

We demonstrate high-performance self-aligned $In_{0.53}Ga_{0.47}As$-channel MOSFETs with effective channel length L_{EFF} down to 20 nm, peak transconductance G_{MSAT} over 2200 μS/μm at L_{EFF} = 30 nm and supply voltage V_{DD} = 0.5 V, thin inversion oxide thickness T_{INV} = 1.8 nm, and low series resistance R_{EXT} = 270 ohm.um. These MOSFETs operate within 20% of the ballistic limit for L_{EFF} < 30 nm and are among the best $In_{0.53}Ga_{0.47}As$ FETs in literature. We investigate the effects of channel/barrier doping on FET performance and show that increase in mobility beyond ~ 500 cm^2/Vs has progressively smaller impact as L_{EFF} is scaled down. Our self-aligned MOSFETs were fabricated using a CMOS-compatible process flow that includes gate and spacer formation using RIE, source/drain extension (SDE) implantation, and in-situ-doped raised source/drain (RSD) epitaxy. This process flow is manufacturable and easily extendable to non-planar architectures.

10:20 a.m.
25.4 Low Power III-V InGaAs MOSFETs Featuring InP Recessed Source/Drain Spacers with Ion=120 μA/μm at Ioff=1 nA/μm and VDS=0.5V, C. Huang, S. Lee, V. Chobpattana, S. Stemmer, A. Gossard, B. Thibeault, W. Mitchell and M. Rodwell, University of California, Santa Barbara

We report low-leakage InGaAs MOSFETs with gate lengths as small as 22 nm. Thinning the InGaAs channel from 4.5 nm to 3 nm allows low I_{off} (1 nA/μm at VDS=0.5V), but degrades the transconductance. Using instead a 4.5 nm InGaAs channel with a 5 nm partially recessed InP spacer, I_{off} is reduced to 1 nA/μm at 45 nm Lg. At 60nm L_g, devices with a 5

nm InP spacer show a high 120 μA/μm on-state current I_{on} at I_{off}=1 nA/μm and VDS=0.5V. This high $1.2*10^5$ on-off ratio in a short L_g device demonstrates the potential for III-V MOSFETs in general-purpose (GP) applications.

10:45 a.m.
25.5 InGaAs/InAs Heterojunction Vertical Nanowire Tunnel TFETs Fabricated by a Top-down Approach, X. Zhao, A. Vardi and J. del Alamo, Massachusetts Institute of Technology

We demonstrate for the first time InGaAs/InAs heterojunction single nanowire (NW) vertical tunnel FETs fabricated by a top-down approach. Using a novel III-V dry etch process and gate-source isolation method, we have fabricated 50 nm diameter NW TFETs with a channel length of 60 nm and EOT=1.2 nm. Thanks to the insertion of an InAs notch, high source doping, high-aspect ratio nanowire geometry and scaled gate oxide, an average subthreshold swing (S) of 72 mV/dec at V_{ds}= 0.5 V is obtained over 2 orders of magnitude of current. On the same device, I_{on}= 0.27 μA/μm is extracted at V_{dd}= 0.3 V with a fixed I_{off}= 10-4 μA/μm. This is the highest ON current demonstrated at this OFF current level in NW TFETs with III-V materials.

11:10 a.m.
25.6 $In_{0.17}Al_{0.83}N$/AlN/GaN Triple T-shape Fin-HEMT with g_m=646 mS/mm, I_{on}=1030 mA/mm, I_{off}=1.13 μA/mm, SS=82 mV/dec and DIBL=28 mV/V at V_D=0.5 V, S. Arulkumaran, N. G. Ing, C. M. M. Kumar, K. Ranjan, K.L. Teo, O. F. Shoron*, S. Rajan*, S. B. Dolmanan** and S. Tripathy**, Nanyang Technological University, *The Ohio State University, **Institute of Materials Research and Engineering

We introduce a novel device structure which incorporates stress engineering technique to achieve simultaneously high performance in on-current (I_{on}), off-current (I_{off}), extrinsic transconductance (gm), SS and DIBL for high speed device applications. The 3D Triple 170-nm T-gate InAlN/GaN 200-nm nano-channel (NC) Fin-HEMTs achieved record high performances of Ion=1.03 A/mm, g_m=645 mS/mm, I_{off}=1.13 μA/mm, SS=82 mV/dec and DIBL=28 mV/V at V_D=0.5 V. Our device uses more relaxed device geometries e.g. 170 nm T-shape-gate versus other reported devices with 70 to 80-nm I-shape-gate on 88-nm fins. So far, this is the first report of T-shape-gate approach on GaN based Fin-HEMTs. The measured Q-factor (gm/SS) of NC Fin-HEMT is 7.9 at V_D=0.5V. Because of these promising electrical transport properties, the proposed 3D Triple T-gate InAlN/AlN/GaN NC Fin-HEMTs on Si are promising for future ultra-high speed device applications.