Session 21: Modeling and Simulation – Atomistic Modeling of Device Interfaces and Materials
Tuesday, December 16, 2:15 p.m.
Imperial Ballroom A
Co-Chairs: Jeffrey Johnson, IBM
Blanka Magyari-Kope, University of Stanford

2:20 p.m.
21.1 On the Microscopic Structure of Hole Traps in pMOSFETs, T. Grasser, W. Goes, Y. Wimmer, F. Schanovsky, G. Rzepa, M. Waltl, K. Rott*, H. Reisinger*, V. Afanas'ev**, A. Stesmans**, A.-M. El-Sayed*** and A. Shluger***, TU Wien, *Infineon, **KU Leuven, **UCL

Hole trapping in the gate insulator of pMOS transistors has been linked to a wide range of detrimental phenomena, including random telegraph noise (RTN), 1/f noise, negative bias temperature instability (NBTI), stress induced leakage currents (SILC) and hot carrier degradation. Since the dynamics of hole trapping appear similar in various oxides such as pure SiO_2, SiON, and high-k, the responsible defects should have a related microscopic structure. While a number of defects have been suspected to be responsible for these phenomena, such as oxygen vacancies/*E'* centers, K centers, hydrogen bridges or hydrogen-related defects in general, the chemical nature of the dominant charge trap remains controversial. Based on extended time-dependent defect spectroscopy (TDDS) data, we investigate the statistical properties of a number of defect candidates using density functional theory (DFT) calculations. Our results suggest that the hydroxyl Ep center is a very likely candidate.

2:45 p.m.
21.2 Analytical Formulation of SiO_2-IL Scavenging in $HfO_2/SiO_2/Si$ Gate Stacks: A Key is the SiO_2/Si Interface Reaction, X. Li, T. Yajima, T. Nishimura, K. Nagashio and A. Toriumi, The University of Tokyo

The scavenging kinetics of ultra-thin SiO_2-IL in HfO_2/ SiO_2/Si stacks is investigated by focusing on SiO_2/Si interface reaction in addition to both O and Si atom kinetics. SiO_2/Si interface serves as a stage that the oxygen vacancy is converted to Si release from SiO_2 with the help of Si substrate. Based on diffusion kinetics and possible reaction, an analytical model for SiO_2-IL scavenging in high-k gate stack is proposed.

3:10 p.m.
21.3 First Principles Study of SiC/SiO_2 Interfaces Towards Future Power Devices, K. Shiraishi, K. Chokawa*, H. Shirakawa*, K. Endo and K. Kamiya**, Nagoya University,*University of Tsukuba, **Kanagawa Institute of Technology

We clarify the intrinsic problems of SiC/ SiO_2 interfaces by the first principles calculations. The unique nearly free electron like characteristics of SiC conduction band bottom causes unexpected formation of interface states near the conduction band bottoms by process induced strain. These results indicate that strain free process is necessary for fabricating high quality NMOSFET. Another proposal is developing PMOSFET instead of presently popular NMOSFET.

3:35 p.m.
21.4 New Framework for the Random Charging/Discharging of Oxide Traps in HfO_2 Gate Dielectric: Ab-initio Simulation and Experimental Evidence, J. Ji, Y. Qiu, S. Guo, R. Wang, P. Ren, P. Hao and R. Huang, Peking University

In this paper, a new framework for first-principle simulation on random charging/discharging of individual oxide traps is established and adopted for detailed studies on HfO_2 high-k gate dielectrics for the first time. The proposed framework provides an effective solution to the challenges in conventional MP simulation methodology, and successfully explains various experimental results in HfO_2 devices. 1-DOV, instead of traditionally assumed SOV, is found to be the crime oxide hole trap in HfO_2. And the anomalous RTN observations strongly support the high-order four-state model, which can be well explained by the two metastable states found in the 2-DOV defect. The framework is helpful for the fundamental understanding of RTN and NBTI reliability.

4:00 p.m.
21.5 Microscopic Understanding of the Low Resistance State Retention in HfO_2 and HfAlO Based RRAM, B. Traoré, P. Blaise, E. Vianello, H. Grampeix, A. Bonnevialle*, E. Jalaguier, G. Molas, S. Jeannot*, L. Perniola, B. De Salvo and Y. Nishi**, CEA, LETI, MINATEC, *STMicroelecteronics, **Stanford University

We study in detail the impact of alloying HfO_2 with Al on RRAM device characteristics through materials characterization, electrical measurements and atomistic simulation. Indeed, movements of individual oxygen atoms inside the dielectric are at the heart of RRAM operations. Therefore, we performed diffusion barrier calculations relative to the oxygen vacancy (Vo) movement involved in Ron data retention. Calculations are performed at the best level using ab initio techniques. Our study provides an insight on the improved Ron stability of HfAlO based RRAM, via a simple explanation based on its higher atomic density (atoms/cm3) associated with shorter bond lengths between cations and anions in the presence of Al.