Session 20: Characterization, Reliability and Yield – Characterization and Reliability of Advanced Devices
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 7-9
Co-Chairs: Benjamin Kaczer, imec
Mikael Casse, CEA LETI

2:20 p.m.
20.1 Low-Frequency Noise and RTN on Near-Ballistic III-V GAA Nanowire MOSFETs, N. Conrad, M. Si, S. H. Shin, J. J. Gu, J. Zhang, M. A. Alam and P. D. Ye, Purdue University

InGaAs has been considered as one of the promising channel materials for CMOS logic circuit because of its large electron injection velocity . InGaAs gate-all-around (GAA) MOSFETs have been demonstrated which offer large drive current and excellent immunity to short channel effects down to deep sub-100 nm channel length. On the other hand, low frequency noise and random telegraph noise (RTN) become more critical as channel length (Lch) scaling down. Meanwhile, traditional oxide characterization methods, such as C-V method and charge pumping method, become impossible due to the extremely small dimensions. Therefore, noise and RTN characterizations become an important approach to quantitatively analyze highly scaled device performance, variability and reliability. Currently, the observation of RTN on bottom-up synthesized long-channel InAs nanowire MOSFETs has been reported. However, there is no any report on RTN and low frequency noise studies of highly scaled III-V GAA MOSFETs by top-down approach. In this work, we (i) report the first observation of RTN on top-down fabricated InGaAs GAA MOSFETs, (ii) examine the origin of low frequency noise on highly scaled InGaAs GAA MOSFETs, (iii) systematically studied low frequency noise and RTN characteristics on near-ballistic InGaAs GAA nanowire MOSFETs.

2:45 p.m.
20.2 RTN and PBTI-induced Time-Dependent Variability of Replacement Metal-Gate High-k InGaAs FinFETs, J. Franco, B. Kaczer, N. Waldron, Ph.J. Roussel, A. Alian, M.A. Pourghaderi, Z. Ji, T. Grasser*, T. Kauerauf, S. Sioncke, N. Collaert, A. Thean and G. Groeseneken**, imec, *T.U. Wien, **also at ESAT, KU Leuven

We study RTN and PBTI in nanoscale InGaAs FinFETs on 300mm Si wafers. The mean instability is found to be identical to planar structures, but significantly larger as compared to Si devices. Although the novel devices follow the same time-dependent variability statistics and the corresponding area-scaling a their Si counterparts, a larger stochastic impact of single defects on the device characteristic is found to induce larger aging-related variance. We ascribe this to more percolative channel conduction induced by still excessive interface and channel defectivity.

3:10 p.m.
20.3 Direct Observation of Self-heating in III-V Gate-all-around Nanowire MOSFETs, S.H. Shin, M. Masuduzzaman, M. Wahab, J. Gu, M. Si, P. D. Ye and M. Alam, Purdue University

Multi-gate devices, such as, FinFET, Gate-all-around transistors (GAA-FET) improve 3D electrostatic control of the channel, but the corresponding increase in self-heating may compromise both performance and reliability. Although the self-heating effect (SHE) of FinFET appears significant, but tolerable, the same may not be true for GAA geometry, especially in quasi-ballistic regime where hot spots and non-classical heat-dissipation pathways may lead to localized damage. The existing reports of the SHE on the SOI, FinFET or GAA-FET have so far relied either on indirect electrical measurements with inherent temporal delays, or on optical infra-red (λ>1.5μm) imaging that cannot resolve deep sub-micron features. As a result, it has so far been impossible to resolve the spatio-temporal features of SHE fully. In this paper, we develop an ultra-fast, high resolution thermo-reflectance (TR) imaging technique to (i) directly observe the local temperature rise of GAA-FET with different number of nanowires (NW), (ii) characterize/interpret the time constants of heating and cooling through high resolution transient measurements, (iii) identify critical paths for heat dissipation, and (iv) detect in-situ time-dependent breakdown of individual NW.

3:35 p.m.
20.4 Gated and STI Defined ESD Diodes in Advanced Bulk FinFET Technologies, S.-H. Chen, D. Linten, J.-W. Lee*, M. Scholz, G. Hellings, A. Sibaja-Hernandez, R. Boschke**, M.-H. Song*, S. Yee*, G. Groeseneken** and A. Thean, imec, *TSMC, ** also at ESAT Department, KU Leuven

The purpose of this work is to study the influence of the process options, such as self-aligned double patterning (SADP), epitaxial re-growth on source/drain (S/D), and local interconnect (LI) with silicide last process, on ESD diode

characteristics in a state-of-the-art bulk FinFET technology. The device characteristics of two different ESD protection diodes, a gated diode and an STI diode, are presented. 3D TCAD simulations are used to bring an in-depth understanding on the current conduction in the ESD protection diodes. The STI diode is the better ESD protection device in the advanced bulk FinFET technology due to the excellent It2/C ratio, compared to the gated diode. Its higher Ron can be partially compensated by enlarging diode width or by rotating the diode orientation. Finally, the proposed wide LI architecture can boost the *It2* with 80% for the ESD protection diodes.

4:00 p.m.
20.5 Study of the Piezoresistive Properties of NMOS and PMOS Omega-Gate SOI Nanowire Transistors: Scalability Effects and High Stress Level, J. Pelloux-Prayer, M. Cassé, S. Barraud, P. Nguyen*, M. Koyama**, Y. Niquet***, F. Triozon, I. Duchemin**, A. Abisset**, A. Idrissi-Eloudrhiri, S. Martinie, J. Rouvière**, H. Iwai*** and G. Reimbold, *CEA-Leti, CEA-Leti and SOITEC, **CEA-Leti and Tokyo Institute of Technology, ***CEA INAC

We hereby present a comprehensive study of piezoresistive properties of aggressively scaled MOSFET devices. For the first time, the evolution of the piezoresistive coefficients with scaled dimensions is presented (gate length down to 20nm and channel width down to 8nm), and from the low to high stress regime (above 1GPa). We have shown that the downscaling of geometrical parameters doesn't allow the use of the conventional definition of piezoresistivity tensor elements. The obtained results give a comprehensive insight on strain engineering ability in aggressively scaled CMOS technology.

4:25 p.m.
20.6 Reliability Challenges for the 10nm Node and Beyond (Invited), J. Stathis, M. Wang, R. Southwick, E. Wu*, B. Linder, E. Liniger, G. Bonilla and H. Kothari, IBM, *STMicroelectronics

Technology elements for the 10nm node and beyond include FINFETs on bulk or SOI, replacement gate process, multi-workfunction gate stacks, self-aligned contacts, and alternative channel materials. New statistical models and improved physics understanding can enable us to anticipate the effects of scaling on reliability even in early stages of development.

4:50 p.m.
20.7 Will Reliability Limit Moore's Law? (Invited), A. Oates, TSMC

Moore's law continues to the engine of growth for the global electronics industry. The understanding of IC degradation mechanisms has resulted in rapid reliability improvements that have enabled the rapid rate technology progression we have experienced. Going forward it is clear that the reliability margins the industry has enjoyed in the past will shrink. The question is now whether reliability will pose a constraint on Moore's law. In this talk we will discuss reliability issues that can most directly impact the industry's capability to maintain the pace of technology progression required by Moore's law.