Session 19: Memory Technology – MRAM, DRAM and NAND
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 6
Co-Chairs: Tao-Cheng Lu, Macronix
Joseph Wang, Qualcomm

2:20 p.m.
19.1 Co/Ni Based p-MTJ stack for sub-20nm High Density Stand Alone and High Performance Embedded Memory Application, G. S. Kar, W. Kim, T. Tahmasebi, J. Swerts, S. Mertens, N. Heylen and T. Min, imec

Excellent tunnel magneto resistance (TMR) values of 143% at resistance-area products (RA) of 4.7 μm^2 from 11nm thin Co/Ni based perpendicular magnetic tunnel junctions (p-MTJ) was achieved. Engineered wetting layer (WL), seed layer (SL) and the introduction of newly designed inner synthetic anti-ferromagnetic pinned layer (iSAF) in combination with ultra-smooth bottom electrode (roughness 0.5 A) was yielded to vertically scaled 11nm thick Co/Ni p-MTJ stack. The introduction of iSAF layer demonstrates for the 1st time the free layer offset field controllability (< 100 Oe) of the spin-transfer-torque (STT) magnetic random access memory (MRAM) device down to 12 nm in diameter.

2:45 p.m.
19.2 Challenging Issues for Tera-bit-level Perpendicular STT-MRAM, J.-G. Park, T.-H. Shim, K.-S. Chae*, D.-Y. Lee, Y. Takemura, S.-E. Lee, M.-S. Jeon, J.-U. Baek, S.-O. Park** and J.-P. Hong, Hanyang University, *Hanyang University & Samsung Electronics Co., Ltd, **Samsung Electronics Co., Ltd.

For realizing terra-bit-level p-STT MRAM to overcome the physical limit of DRAM, perpendicular-magnetic tunnel junctions (p-MTJs) challenge to satisfy critical parameters such as a high tunneling magneto-resistance (TMR) ratio of 150%, thermal stability (Δ) of > 74 at 85°C, a low critical current density (Jc) of 13.4 MA/cm^2, and anti-ferromagnetic-coupling-strength (J_{ex}) for a synthetic anti-ferromagnetic (SyAF) layer of > 0.7erg/cm^2. In particular, four critical parameters for p-MTJs should be simultaneously performed at the back-end-line (BEOL) of > 350°C and 300-mm TiN electrode wafers.

3:10 p.m.
19.3 Area Dependence of Thermal Stability Factor in Perpendicular STT-MRAM Analyzed by Bi-directional Data Flipping Model, K. Tsunoda, M. Aoki, H. Noshiro, Y. Iba, C. Yoshida, Y. Yamazaki, A. Takahashi, A. Hatada, M. Nakabayashi, Y. Tsuzaki and T. Sugii, Low-power Electronics Association and Project (LEAP)

This paper reports the statistical analysis of thermal stability factor for the top-pinned perpendicular MTJ (p-MTJ) array. By using bi-directional data flipping model, data retention characteristics of "0" and "1" states can be fitted separately including saturation of failure probability. As a result, it became clear that the thermal stability factor of "1" state increases as the device area increases, whereas that of "0" state remains constant regardless of the size. Moreover, we found that the p-MTJ exhibits much smaller variation of thermal stability factor (9.6~14.3%) in comparison with the in-plane MTJ. Variations of thermal stability factor in both states decrease with the increase of the area. By the direct resistance evaluation of the MTJ array, the key parameter to increase the thermal stability factor and suppress its variation was investigated.

3:35 p.m.
19.4 0.026μm^2 High Performance Embedded DRAM in 22nm Technology for Server and SOC Applications, C. Pei*, G. Wang, M. Aquilino, N. Arnold, B. Chandra, W. Chang, X. Chen, W. Davies, K. Hawkins, D. Jaeger, J. B. Johnson#, O.-J. Kwon, R. Krishnasamy#, W. Kong, J. Liu, X. Li, B. Messenger, E. Nelso, K. Nummy, K. Onishi, D. Poindexter, S. Rombawa, C. Sheraw, T. Tzou, X. Wang, M. Yin, G. Freeman, T. Kirahata, E. Maciejewski, J. Norum, , N. Robson, S. Narasimha, P. Parries, P. Agnello, R. Malik and S.S. Iyer, IBM Semiconductor Research and Development Center

This paper presents the industry's smallest eDRAM based on IBM's 22nm SOI technology. With cell dimensions shrinking, critical issues for eDRAM such as n-band resistance, junction butting, parasitic adjacent DT-induced leakage (PADIL), gate induced drain leakage (GIDL) and Vt variation present have been discussed and innovations were needed to address these issues. This paper summarizes the n-band resistance innovations, and reports for the first time the asymmetric embedded stressor, cavity implant and through gate implant employed in 22nm eDRAM technology. The 22nm eDRAM has various applications on IBM's server chips as on-chip embedded caches as well as associated

applications. The fully integrated 256Mb product array has demonstrated capability of 1.4ns cycle time, which is significantly faster than any other embedded DRAM. We have achieved latency of 700 ps for certain cache instantiations, which is faster than SRAM for those sizes. 22nm eDRAM has been recently leveraged for IBM's 12-core 649mm^2 Server Processor POWER8™.

4:00 p.m.
19.5 A New Saw-Like Self-Recovery of Interface States in Nitride-Based Memory Cell, Y.-T. Sung, P.-Y. Lin, J. Chen, T.-S. Chang, Y.-C. King and C. J. Lin, National Tsing Hua University, Taiwan Semiconductor Manufacturing Company

A new saw-like self-recovery Self-Aligned Nitride (SAN) memory cell is proposed and fabricated in 28nm high-k metal gate (HKMG) CMOS process for high-density logic NVM applications. The cell is operated with Source-Side Injection (SSI) for programming and band-to-band hot holes (BBHH) for erasing. Two effective self-heating recovery mechanisms are proposed and performed to maintain a stable On/Off read window after cycling stresses. Besides, the characteristic and reliability comparison of the SAN cell in other technology nodes, 90nm/45nm/32nm, are characterized to further verify the saw-like self-detrapping and self-recovery operation. The new 28nm HKMG SAN memory cell with the self-detrapping recovery results excellent and superior endurance performance and can provide a very promising solution for logic NVM in advanced technologies.

4:25 p.m.
19.6 A Novel Double-Trapping BE-SONOS Charge-Trapping NAND Flash Device to Overcome the Erase Saturation without Using Curvature-Induced Field Enhancement Effect or High-K (HK)/Metal Gate (MG) Materials, H.-T. Lue, R. Lo, C.-C. Hsieh, P.-Y. Du, C.-P. Chen, T.-H. Hsu, K.-P. Chang, Y.-H. Shih and C.-Y. Lu, Macronix International Co.

Erase saturation issue is a fundamental challenge for SONOS-type charge-trapping NAND Flash devices. Nowadays the most popular way to solve this issue is to pursue either curvature-induced field enhancement effect in the nano-wire SONOS device, or HK/MG to suppress the gate injection. However, both approaches have its drawback and reliability challenges. In this work, we propose a completely different approach that utilizes a double-trapping (or double storage) layer in a barrier engineered (BE) SONOS device to overcome the erase saturation ideally. A second nitride trapping layer (N3) is stacked on top of the first blocking oxide (O3) and 1st trapping layer (N2) of the original BE-SONOS device. Both theoretical model and experimental measured results indicate that when N3 stores sufficient electron charge it can greatly suppress gate injection, allowing continuous hole injection into N2 that gives a very deep erased Vt ~ -6V. A fully-integrated 3D Vertical Gate (VG) NAND Flash test chip using this novel device has been fabricated which demonstrates excellent MLC operation window and reliability. The flat and planar topology of this double-trapping BE-SONOS device enables minimal design rule of 3D NAND Flash array and possesses superb read disturb immunity.