Session 18: Circuit Device Interaction – Analog and Mixed Signal Circuit Device Interaction
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 5
Co-Chairs: Ru Huang, Peking University
Peter Rickert, Texas Instruments

2:20 p.m.
18.1 Device Aware High-Speed Transceiver Design in Planar and FinFet Technologies, K. Chang, J. Savoj, P. Upadhyaya and Y. Frans, Xilinx Inc.

This paper studies the interaction between devices and analog circuits used in high-speed transceivers in both planar and FinFet processes. It describes the impact of variations on the design of both active and passive devices, and devises circuit techniques to mitigate their impact on the performance of transceivers. Case studies of transceiver components in 20nm planar and 16nm FinFET processes are used to illustrate the interactions. With proper design techniques, the transceiver in 20nm operates up to 16.3Gb/s. Figure 10(a) shows the 28dB channel used for the testing for 20nm transceiver [1]. The resulting transmitter random jitter (RJ) is 313fs, shown in Figure 10(b). The LC PLL covers from 8Gb/s-16.3Gb/s without frequency dividers. Figure 10(c) shows the receiver eye opening via eye scan result and Figure 10(d) shows the measured bit error rate is lower than 10-15 over the 28dB channel. The robust performance validates all the circuit techniques used for the advanced process nodes.

2:45 p.m.
18.2 Mismatch in High-K Metal Gate Process Analog Design, A. Woo, H. Eberhart, Y. Li and A. Ito, Broadcom Corporation

This paper presents mismatch behaviors of high-K metal gate transistors when used in analog design applications. The data collected shows the sensitivity of mismatch in the high-K metal gate process to the overall layout environment, including top metal routing placement, which was not reported before this work. We compared data from different fabrication sources which indicated that mismatch can be improved through process as well as through layout strategy.

3:10 p.m.
18.3 Challenges of Analog and I/O Scaling in 10nm SoC Technology and Beyond, A. Wei, J. Singh, I. Chakarov, G. Bouche, J. Stephens, I. Lin, U. Schroeder, M. Rashed, J. Kye, L. Yuan, Y. Woo, J. Zeng, H. Levinson, A. Wehbi, P. Hang, V. Ton-That, V. Kanagala, D. Yu, D. Blackwell, M. Sureddin, A. Beece, S. Gao, S. Thangaraju, R. Alapati, S. Samavedam, GLOBALFOUNDRIES

Analog/mixed signal and I/O area of the SoC is projected to increase at a faster rate due to overscale of digital blocks to keep up with Moore's Law cost scaling. The challenges of analog I/O scaling are described. 3-D TSV is shown to be a very good option to maintain or exceed cost scaling in the next technology nodes.

3:35 p.m.
18.4 Technology Pathfinders for Low Cost and Highly Integrated RF Front End Modules, C. Raynaud, CEA-LETI

The focus of this paper is to highlight the challenges related to the increasing number of modes (GSM, WCDMA, LTE..) and frequency bands in mobile devices. It describes the technology pathfinders to get cheaper highly integrated multi-mode multi–band RF Front End modules.

4:00 p.m.
18.5 Digitally-Intensive RF Transceivers in Highly Scaled CMOS, C.-M. Hung, MediaTek Inc.

Fast transistors and increasing device non-ideality in advanced nodes have motivated the development of digitally-intensive RF systems which have become ubiquitous using algorithms with thousands of control signals to combat with exacerbated analog impairments. In this paper, we will explore the power of embedded intelligence which greatly reduces the sensitivity of circuit performance to device characteristics. There are still constraints mandating device-level enhancement. Strong interactions between circuit and device communities are required to accomplish competitive products.

4:25 p.m.

18.6 Circuit and Device Interactions for 3D Integration Using Inductive Coupling, T. Kuroda, Keio University

This paper presents a ThruChip Interface using inductive coupling. Reliability data is measured. Application, manufacturability, and scaling scenario are discussed.