Session 17: Power and Compound Semiconductor Devices – Trapping Mechanisms in AlGaN/GaN Transistors
Tuesday, December 16, 2:15 p.m.
Continental Ballroom 4
Co-Chairs: Subramaniam Arulkumaran, Nanyang Technological University
Michael Uren, University of Bristol

2:20 p.m.
17.1 The Dynamics of Surface Donor Traps in AlGaN/GaN MISFETs using Transient Measurements and TCAD Modelling, G. Longobardi, F. Udrea, S. Sque*, J. Croon*, F. Hurkx* and J. Šonský*, Cambridge University, *NXP Semiconductors

A dynamic analysis of surface donor traps in AlGaN/GaN MISFETs has been carried out using Id-Vg, Cgg(V), and transient measurements and TCAD simulations. For the first time we were able to explain in details the physical mechanisms of the transient charge transport between the donor traps and the 2DEG layer.

2:45 p.m.
17.2 Thermally Induced Threshold Voltage Instability of III-Nitride MIS-HEMTs and MOSC-HEMTs: Underlying Mechanisms and Optimization Schemes, S. Yang, S. Liu, C. Liu, Z. Tang, Y. Lu and K. J. Chen, The Hong Kong University of Science and Technology

The mechanisms of divergent V_{TH}-thermal-stability in MIS-HEMTs and MOS-Channel-HEMTs have been revealed. The more significant V_{TH}-thermal-instability in MIS-HEMTs originates from the polarized barrier layer that separates the dielectric/GaN interface from the channel, allowing "deeper" interface trap levels crossing the Fermi level during the device's turn-on. Normally-off MIS-HEMTs with optimized performance/stability trade-offs are thereby demonstrated.

3:10 p.m.
17.3 Impacts of Fluorine-treatment on E-mode AlGaN/GaN MOS-HEMTs, X. Sun, Y. Zhang, K. Chang-Liao, T. Palacios* and T. Ma, Yale University, *Massachusetts Institute of Technology, **National Tsing Hua University

The impact of fluorine treatment on AlGaN/GaN MOS-HEMTs has been investigated. Fluorine was found to suppress pre-existing donor-traps in MOS-HEMT, which improves the off-state at high temperatures. Fluorine doping/etch, however, also generates slow border traps and fast interface states that degrade the MOS-HEMT performance.

3:35 p.m.
17.4 High-Temperature Low-Damage Gate Recess Technique and Ozone-Assisted ALD-grown Al_2O_3 Gate Dielectric for High-Performance Normally-Off GaN MIS-HEMTs, S. Huang, Q. Jiang*, K. Wei, G. Liu, J. Zhang, X. Wang, Y. Zheng, B. Sun, C. Zhao, H. Liu, Z. Jin, X. Liu, H. Wang*, S. Liu*, Y. Lu*, C. Liu*, S. Yang*, J. Zhang**, Y. Hao** and K. J. Chen*, Chinese Academy of Sciences, *The Hong Kong University of Science and Technology, **Xidian University

A high-temperature gate recess technique featuring low damage and in-situ self-clean capability, in combination with ozone-assisted ALD growth of Al_2O_3 gate dielectric, is developed for fabrication of GaN-based normally-off power devices. High performance normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs featuring high drive current, low specific ON-resistance, and low current collapse, are achieved.

4:00 p.m.
17.5 Trapping and High Field Related Issues in GaN Power HEMTs, G. Meneghesso, M. Meneghini, A. Chini*, G. Verzellesi** and E. Zanoni, University of Padova, *Enzo Ferrari, **University of Modena and Reggio Emilia

Gallium Nitride HEMTs devices grown on Si substrates are the most promising solution for the future technologies in the power electronics industry. Compensation of unintentional GaN n-type conductivity is specifically mandatory in the buffer for an optimum device blocking function. Carbon (C) or Iron (Fe) doping are the most common solutions that however are responsible also for the introduction of traps in the buffer, that induces large charge trapping and current collapse when devices are biased at high voltages as well as affect breakdown behavior of these devices. This paper review the main high field related issues recently reported in GaN-on-Si devices for power applications.

4:25 p.m.

17.6 CMOS-Compatible GaN-on-Si Field-Effect Transistors for High Voltage Power Applications, M.-H. Kwan, K.-Y. Wong, F. W. Yao, M. W. Tsai, Y. S. Lin, Y.-C. Chang, P. C. Chen, R. Y. Su, J. L. Yu, F. J. Yang, G. P. Lansbergen, M.-C. Lin, T. C. Lin, H.-Y. Wu, P.-C. Liu, C.-M. Chen, T. C. Y. Yu, C. B. Wu, B. Lin, M.-H. Chang, S.-P. Wang, L.C. Chen, Tom Tsai, H.C. Tuan and Alex Kalnitsky, TSMC

CMOS-compatible 100/650V enhancement-mode FETs and 650V depletion-mode MISFETs are fabricated on 6-inch AlGaN/GaN-on-Si wafers. They show high BV and low specific Ron with good wafer uniformity. The importance of epitaxial quality is figured out in a key industrial item: high-temperature-reverse-bias-stress-induced on-state Id degradation. Optimization of epitaxial layers shows significant improvement of device reliability.