Session 16: Nano Device Technology – Ge and SiGe Transistorts
Tuesday, December 16, 2:15 p.m.
Grand Ballroom A
Co-Chairs: Matthias Passlack, TSMC
Shinichi Takagi, University of Tokyo

2:20 p.m.
16.1 First Demonstration of High-Ge-Content Strained-Si1$_{-x}$Ge$_x$ (x=0.5) on Insulator PMOS FinFETs with High Hole Mobility and Aggressively Scaled Fin Dimensions and Gate Lengths for High-Performance Applications, P. Hashemi, K. Balakrishnan, S. Engelmann, J.A. Ott, A. Khakifirooz, A. Baraskar, M. Hopstaken, J.S. Newbury, K. Chan, E. Leobandung, R. Mo and D.G. Park, IBM, GLOBALFOUNDRIES

For the first time, we report fabrication and characterization of high-performance s-Si$_{1-x}$Ge$_x$-OI (x~0.5) pMOS FinFETs with aggressively scaled dimensions. We demonstrate realization of s-SiGe fins with W_{FIN} =3.3nm and devices with LG=16nm, in a CMOS compatible process. Using a Si-cap-free passivation process, we report SS=68mV/dec and μ_{eff}=390±12 cm^2/Vs at N_{inv}=1e13 cm^{-2}, outperforming the state-of-the-art relaxed Ge FinFETs. We also report the highest performance reported to date among sub-20nm-L_G pMOS FinFETs at VDD=0.5V. In addition, hole transport as well as electrostatics, performance and leakage characteristics of SGOI FinFETs for various dimensions are comprehensively studied in this work.

2:45 p.m.
16.2 Dual-Channel CMOS Co-Integration with Si Channel NFET and Strained-SiGe Channel PFET in Nanowire Device Architecture Featuring 15nm Gate Length, P. Nguyen*, S. Barraud*, C. Tabone*, L. Gaben*^, M. Cassé*, F. Glowvacki*, J.-M. Hartmann*, M.-P. Samson^, V. Maffini-Alvarro*, C. Vizioz*, N. Bernier*, C. Guedj*, C. Mounet*, O. Rozeau*, A. Toffoli*, F. Allain*, D. Delprat**, B.-Y. Nguyen**, C. Mazuré** and O. Faynot*, M. Vinet*, *CEA-LETI, ^ STMicroelectronics, **SOITEC

For the first time, we have fabricated hybrid channel omega-gate CMOS nanowire (NW) with strained SiGe-channel (cSiGe) p-FETs and Si-channel n-FET. An optimized process flow based on the Ge enrichment technique results in a +135% hole mobility enhancement at long gate lengths compared to Si. Effectiveness of cSiGe channel is also evidenced for ultra-scaled p-FET NW (LG=15 nm) with +90% ION current improvement. [110]-oriented NW is shown to be the best candidate to improve drive current under compressive strain. In this work, the strain is measured by using precession electron diffraction with a 1nm spatial resolution. Furthermore, we show that hybrid integration reduces the delay of CMOS ring oscillator (FO=3) by 50% at VDD=0.9V. Finally, we demonstrate the most aggressively scaled hybrid CMOS NWs reported to date with NW width and gate length down to 7nm and 11nm, while maintaining high drive current (687µA/µm for p-FET and 647µA/µm for n-FET) with low leakage current and excellent short-channel-control (DIBL<50mV/V).

3:10 p.m.
16.3 Vth Adjustable Self-aligned Embedded Source/drain Si/Ge nanowire FETs and Dopant-free NVMs for 3D Sequentially Integrated Circuit, C.-C. Yang, T.-Y. Hsieh, W.-H. Huang, H.-H. Wang, C.-Y. Chen*, K.-S. Chang-Liao* and J.-M. Shieh, National Nano Device Laboratories, *National Tsing Hua University

3D stackable high-performance Si nanowire field-effect transistors (NWFETs) and dopant-free Ge junctionless nanowire non-volatile memories (JL-NWNVMs) with self-aligned embedded source/drain (e-S/D) current boosters and independent back gate (BG) Vth adjusters for 3D sequential integrated circuit are realized at low thermal budget process (<450°C). The fabricated Si NWFETs exhibit low subthreshold swings (96 and 125 mV/dec.), high on-currents (232 and 110 µA/µm), and large γ value (>0.05) for V_{th} adjustment. The high-k capped blocking dielectric bandgap engineered dopant-free Ge JL-NWNVM exhibits high I_{on}/I_{off} ratio (>1E5), large memory window (>4V), and low charge loss (<40%, 10yrs). Thanks to the quantum confinement effect, such Vth adjustable nanowire devices perform well at higher temperatures, which give a wide design window for 3D sequential integrated circuit.

3:35 p.m.
16.4 Enhancement Mode Strained (1.3%) Germanium Quantum Well FinFET (WFin=20nm) with High Mobility (uHole=700 cm^2/Vs), Low EOT (~0.7nm) on Bulk Silicon Substrate, A. Agrawal, M. Barth, G. B. Rayner*, V.T. Arun, C. Eichfeld, G. Lavallee, S.-Y. Yu, X. Sang**, S. Brookes**, Y. Zheng, Y.-J. Lee^, Y.-R. Lin^, C.-H. Wu^,

C-H Ko^, J. LeBeau**, R. Engel-Herbert, S. E. Mohney, Y.-C. Yeo^ and S. Datta, The Pennsylvania State University, *Kurt J. Lesker Company, **North Carolina State University, ^Taiwan Semiconductor Manufacturing Company

Compressively strained Ge (s-Ge) quantum well (QW) FinFETs with $Si_{0.3}Ge_{0.7}$ buffer are fabricated on 300mm bulk Si substrate with 20nm WFin and 80nm fin pitch using sidewall image transfer (SIT) patterning process. We demonstrate (a) in-situ process flow for a tri-layer high-κ dielectric $HfO_2/Al_2O_3/GeO_x$ gate stack achieving ultrathin EOT of 0.7nm with low DIT and low gate leakage; (b) 1.3% s-Ge FinFETs with Phosphorus doped $Si_{0.3}Ge_{0.7}$ buffer on bulk Si substrate exhibiting peak μ_h=700cm^2/Vs, μ_h =220 cm^2/Vs at 10^{13} /cm^2 hole density. The s-Ge FinFETs achieve the highest $\mu*C_{Max}$ of $3.1x10^{-4}$ μF/Vs resulting in 5x higher I_{ON} over unstrained Ge FinFETs.

4:00 p.m.

16.5 First Demonstration of 15nm-W_{FIN} Inversion-Mode Relaxed-Germanium n-FinFETs with Si-cap Free RMG and NiSiGe Source/Drain, J. Mitard, L. Witters, H Arimura, Y. Sasaki, A.P. Milenin, R. Loo, A. Hikavyy, G. Eneman, P Lagrain, H. Mertens, S. Sonja, C. Vrancken, H. Bender, K. Barla, N. Horiguchi, A. Mocuta, N. Collaert and A. Thean, imec

This work demonstrates the feasibility of an inversion-mode relaxed Ge n-FinFET scaled down to 15-nm fin width and sub-40-nm gate length. CMOS-compatible processing steps such as STI formation, RMG gate stack, raised-SiGe S/D and a Ni-based contact scheme have been successfully implemented. This first industry-compatible Ge n-FinFET has a $G_{M,SAT,EXT}$ / SS_{SAT} of 250 μS.μm^{-1} / 130 mV.dec^{-1} (V_{DS}=0.5V) which is on par with accumulation-mode junction-less Ge n-FETs.

4:25 p.m.

16.6 High-performance tri-gate poly-Ge Junction-less p- and n-MOSFETs Fabricated by Flash Lamp Annealing Process, K. Usuda, Y. Kamata, Y. Kamimuta, T. Mori, M. Koike and T. Tezuka, AIST, Collaborative Research Team Green Nanoelectronics Center (GNC)

High-performance tri-gate poly-Ge junction-less p- and n-MOSFETs on insulator were fabricated by flash lamp annealing (FLA) process. The mobility values were both higher than drift mobility for c-Si with the same carrier concentration. The FLA poly-Ge CMOS will provide great potential for future 3D LSIs.

4:50 p.m.

16.7 Deep Sub-100 nm Ge CMOS Devices on Si with the Recessed S/D and Channel, H. Wu, W. Luo, M. Si, J. Zhang, H. Zhou and P. Ye, Purdue University

We report on comprehensive studies on Ge CMOS devices with the recessed S/D and channel fabricated on the GeOI substrate. Both nFETs and pFETs with channel lengths from 500 to 20 nm, channel thicknesses from 90 to 15 nm, EOTs from 5 to 3 nm and gate stacks with and without the post oxidation (PO) are investigated. Benefiting from the fully depleted ultra-thin channel with a reasonable interface, a low sub-threshold slope (SS) of 95 mV/dec is obtained in a 60 nm L_{ch} nFET and a record high I_{ON}/I_{OFF} ratio of 106 is realized in a 300 nm L_{ch} nFET. The recessed contact strongly dependents on the recessed depth and optimized recessed depth significantly improves the Ge contacts.