Session 14: Characterization, Reliability and Yield – Advanced Memories and TSV
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: Francesco Driussi, Universita di Udine
Su Jin Ahn, Samsung Electronics

9:05 a.m.
14.1 Progressive vs. Abrupt Reset Behavior in Conductive Bridging Devices : a C-AFM Tomography Study, U. Celano, L. Goux, A. Belmonte, G. Giammaria**, K. Opsomer, C. Detavernier*, O. Richard, H. Bender, F. Irrera**, M. Jurczak and W. Vandervorst, imec, *University of Gent, **Università "La Sapienza"

The Conductive bridging device (CBRAM) is considered as a valuable non-volatile storage technology, because it offers fast switching, high endurance and good scalability. CBRAM operation relies on the voltage-induced redox-based formation and rupture of a Cu- or Ag-based conductive filament (CF) in an insulating layer acting as a solid state electrolyte. Whereas the presence of a metallic CF is commonly accepted for the low resistive state (LRS), the conduction nature of the high resistive state (HRS) is less clear. Generally, the formation of the HRS is described as an electrochemical-driven dissolution of the CF leading to a tunnel-barrier formation, a current constriction in a quantum-point-contact (QPC), or conduction by trap-controlled mechanisms. In this paper, for the first time, we report on the observation of the HRS conduction mechanisms (tunneling in a broken filament, current constriction in a QPC) for 1T1R memory elements by mean of C-AFM tomography. Next, we relate the reset-behaviors experimentally observed, to specific configurations of the CF in the LRS.

9:30 a.m.
14.2 Understanding the Impact of Programming Pulses and Electrode Materials on the Endurance Properties of Scaled Ta_2O_5 RRAM Cells, C. Chen, L. Goux, A. Fantini, A. Redolfi, S. Clima, R. Degraeve, Y. Chen, G. Groeseneken and M. Jurczak, imec

We demonstrate strong impact of reset amplitude and duration on endurance degradation of scaled TiN\Ta_2O_5\Ta cells, which from ab-initio and switching simulation is attributed to O interaction with TiN. Clear improvements are obtained using (i) shorter write pulses, (ii) low O-affinity Ru bottom electrode, and (iii) higher O-affinity HfO_2 dielectric.

9:55 a.m.
14.3 Pulsed Cycling Operation and Endurance Failure of Metal-oxide Resistive RAM, S. Balatti, S. Ambrogio, Z.Q. Wang, A. Calderoni*, N. Ramaswamy* and D. Ielmini, Politecnico di Milano, *Micron Technology Inc.

We studied pulsed operation and endurance of oxide RRAM. We show that (i) resistance window (RW) is controlled by the negative voltage Vstop applied during reset, (ii) failure at high Vstop is due to negative set, causing filament overgrowth and RW collapse and (iii) endurance is independent of the pulse-width, which supports an Arrhenius model for endurance failure. Limitation of the current during negative reset is finally demonstrated to improve endurance.

10:20 a.m.
14.4 Impact of Low-frequency Noise on Read Distributions of Resistive Switching Memory (RRAM), S. Ambrogio, S. Balatti, V. McCaffrey*, D. Wang* and D. Ielmini, Politecnico di Milano, *Adesto Technologies

Resistive switching memory (RRAM) is highly promising for future low-power, high-speed, high-density memory technologies. A key concern for RRAM development is given by current fluctuations, which affect retention of single-bit and multilevel memories. We studied current fluctuation (noise) in RRAM at both cell and array levels. We present a model for 1/f and random telegraph noise (RTN) in intrinsic cells, allowing to predict time-dependent broadening of read current (Iread) distributions. Then we address tail cells with large noise in 0.5 Mb arrays, revealing for the first time time-decaying random walk and intermittent RTN. A statistical noise model is developed and discussed.

10:45 a.m.
14.5 A New Approach for Trap Analysis of Vertical NAND Flash Cell using RTN Characteristics, D. Kang, C. Lee, S. Hur, D. Song and J.-H. Choi, Samsung Electronics Co.

We introduce new phenomena that show turn-on at back-side for Vertical NAND (V-NAND) with back-insulator and propose a new method to analyze the trap of back-interface related to the phenomena. Back-side traps have been analyzed with the back-gate structure [1]. However, V-NAND has no back-gate structure, so it's difficult to observe traps. With RTN method we proposed, it's possible for us to observe back-side traps.

11:10 a.m.
14.6 Through Silicon Via (TSV) Effects on Devices in Close Proximity– the Role of Mobile Ion Penetration - Characterization and Mitigation, C. Kothandaraman, S. Cohen, C. Parks, J. Golz, K. Tunga, S. Rosenblatt, J. Safran, C. Collins, W. Landers, J. Oakley, J. Liu, A.J. Martin, K. Petrarca, M. Farooq, T.L. Graves-Abe, N. Robson and S.S. Iyer, IBM Microelectronics

A new interaction between TSV processes and devices in close proximity, different from mechanical stress, is identified, studied and mitigated. Detailed characterization via Triangular Voltage Sweep (TVS) and SIMS shows the role of mobile ion penetration from BEOL layers. An improved process is presented and confirmed in test structures and DRAM.

11:35 a.m.
14.7 Highly Beneficial Organic Liner with Extremely Low Thermal Stress for Fine Cu-TSV in 3D-Integration, M. Murugsan, T. Fukushima, J.C. Bea, Y. Sato, H. Hashimoto, K.W. Lee and M. Koyanagi, Tohoku University

The constructive role played by the physical vapor deposited (PVD) organic polyimide (PI) liner in the Cu-TSVs with ϕ varying from 3 µm to 30 µm has been studied meticulously for its thermal stability, leakage current, capacitance, TSV-chain resistance, stress absorbing ability, and the Si-lattice distortion arising from thermo-mechanical stress (TMS). The I-V data revealed that the leakage current for the PVD deposited PI liner is in the order of 10^{-13} to 10^{-15} A, which is on par with the value obtained for the conventional SiO_2 liner. The extremely low modulus value of PI liner partly accommodates the expanded Cu during heating, and it assits to reduce the vertical Cu extrusion. More importantly, not only the amount of Cu extrusion is reduced nearly one-half to the extrusion amount for conventional liner, but also helps to maintain an uniform Cu-extrusion. We were able to achieve a conformal deposition of PI liner even in ϕ = 3 µm via having the aspect ratio of 10 with the step coverage values of more than 0.8 at the TSV bottom corner. The reciprocal space lattice data obtained for 3D-LSI sample revealed that the Si-lattice structure is heavily distorted in the TSV space region for TSV with SiO_2 liner. It was found that the d-space changing and thus the lattice stress is nearly five times larger for TSV with SiO_2 liner (~1000 MPa) than for the TSV with PI liner (~200 MPa). The observed lattice tilt for 3 µm and 30 µm TSV with PI liner was respectively 0.001 deg. and 0.012 deg. Whereas the lattice tilt obtained for TSV with SiO_2 liner is three order of magnitude larger. Nearly zero-degradation of PI liner was confirmed from C1s, O1s, and N1s core-level x-ray photoelectron spectra taken before and after annealing at 400 ℃. The

presence of hysteresis and the positive shift in Vfb in the C-V curve for the PI liner revealing the presence of negatively charged species, and it may form a cause of problem. We obtained the resistance value of as low as 18 mΩ per 10 µm-width TSV with PI liner fabricated on 12-inch wafer level. Due to the soft nature of PI liner, there appears brindle pattern on the surface of PI liner along with an four fold increase in the surface roughness after annealing at 400 ℃. Irrespective of the TSV size, two dimensional µ-Raman spectroscopic stress analysis revealed the existence of less than 200 MPa of stress in the Si around the TSV with PI liner which is in close agreement with the micro-diffraction results. It is proven that the TMS produced by the Cu-TSVs overlapping both orthogonal and ortho-diagonal, orthogonal only and no-stress overlapping for the respective samples containing TSV with SiO_2 liner, PI on SiO_2 liner, and PI liner alone.