Session 13: Nano Device Technology – Steep-Swing Devices
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: Chen-Hsin Lien, National Tsing Hua University
Katsuhiro Tomioka, Hokkaido University

9:05 a.m.
13.1 NEM Relay Design for Compact, Ultra-Low-Power Digital Logic Circuits, T.-J. King Liu, N. Xu, I-R. Chen, C. Qian and J. Fujiki*, University of California, Berkeley, *Toshiba Corporation

Since mechanical switches (relays) have zero off-state leakage and perfectly abrupt ON/OFF switching behavior, they can be operated with a very small voltage swing and hence are promising for overcoming the energy efficiency limit of CMOS technology. Remaining challenges for realizing the promise of ultra-low-power mechanical computing are further miniaturization to achieve very small device footprint; contact surface adhesion; and process-induced variability. This paper discusses recent developments to surmount these challenges.

9:30 a.m.
13.2 High I_{on}/I_{off} Ge-source Ultrathin Body Strained-SOI Tunnel FETs – Impact of Channel Strain, MOS Interfaces and Back Gate on the Electrical Properties, M. Kim, Y. Wakabayashi, R. Nakane, M. Yokoyama, M. Takenaka and S. Takagi, The University of Tokyo

Ge/strained-Si hetero-junction TFETs with in-situ B doped Ge have been demonstrated. The increase in channel strain and optimization of PMA have successfully realized high performance of steep SSmin below 30 mV/dec and large I_{on}/I_{off} ratio over $3x10^7$.

9:55 a.m.
13.3 Comprehensive Performance Re-assessment of TFETs with a Novel Design by Gate and Source Engineering from Device/Circuit Perspective, Q. Huang, R. Huang, C. Wu, H. Zhu, C. Chen, J. Wang, L. Guo, R. Wang, L. Ye and Y. Wang, Peking University

In this paper, a novel TFET design, called Pocket-mSTFET, is proposed and experimentally demonstrated by evaluating the performance from device metrics to circuit implementation for low-power SoC applications. For the first time, from circuit design perspective, TFETs performance in terms of I_{ON}, I_{OFF}, subthreshold slope (SS), output behavior, capacitance, delay, noise and gain are experimentally benchmarked and also compared with MOSFET. By gate and source engineering without area penalty, the compatibly-fabricated Pocket-mSTFET on SOI substrate shows superior performance with the minimum SS of 29mV/dec at 300K, high I_{ON} (~20μA/μm) and large I_{ON}/I_{OFF} ratio (~10^8) at 0.6V. Largely alleviated super-linear onset issue, reduced Miller capacitance and delay, and much lower noise level were also experimentally obtained, as well as high effective gain. Circuit-level implementation based on Pocket-mSTFET also shows significant improvement on energy efficiency and power reduction at V_{DD} of 0.4V, which indicates great potential of this TFET design for low-power digital and analog applications.

10:20 a.m.
13.4 A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current, J. Zhang, M. De Marchi, P.-E. Gaillardon and G. De Micheli, EPFL

We demonstrate a steep subthreshold slope silicon FinFET with Schottky source/drain. The device shows a minimal SS of 3.4 mV/dec and an average SS of 6.0 mV/dec over 5 decades of current swing. Ultra-low leakage floor of 0.06 pA/μm is also achieved with high Ion/Ioff ratio of 10^7.

10:45 a.m.
13.5 Can Piezoelectricity Lead to Negative Capacitance?, J. Wong and S. Salahuddin, University of California, Berkeley

A thermodynamic model is used to show that pure piezoelectricity and higher-order electromechanical coupling cannot provide a negative capacitance effect.

11:10 a.m.

13.6 Sub-60 mV/decade Steep Transistors with Compliant Piezoelectric Gate Barriers, R. Jana, G. Snider and D. Jena, University of Notre Dame

Introduction: Steep transistors with sub-60 mV/decade subthreshold slope are being actively pursued for ultra-low voltage and low-power nanoelectronic applications1. Transistors with steep switching have been achieved either by modifying conventional drift-diffusion transport mechanism with interband tunneling from the source to the channel [1], or by replacing conventional passive gate dielectrics with active gate barrier materials such as ferroelectrics2, piezoelectrics [3,4,5]. By using a ferroelectric gate insulator of a transistor, it is possible to obtain negative differential capacitance (NDC) in the gate stack that results in an amplification of the internal channel surface potential, ψ_s induced by the applied gate voltage, V_{gs}, leading to an internal voltage gain(1)$/m=(\partial\psi_s)/(\partial V_{gs}>1)$. Owing to voltage gain, the body factor $m=(\partial V_{gs})/(\partial\psi_s)$is reduced below one, i.e. m<1, and hence the subthreshold slope (SS=m×60 mV/decade) can be lowered than 60 mV/decade [2]. Overcoming the subthreshold slope limit by NDC is made possible using a series combination of a negative and a positive capacitance, which makes the total capacitance, looking into the gate, to be larger than the positive capacitance [2]. Therefore, in order to induce the same amount of channel charge, an NDC gate FET would require a smaller gate voltage than a conventional FET.