Session 12: Circuit Device Interaction – Circuit/Device Variability and Integrated Passives Performance
Tuesday, December 16, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: Jan Hoentschel, Globalfoundries
Shyh-Horng Yang, TSMC

9:05 a.m.
12.1 Scaling Breakthrough for Analog/Digital Circuits by Suppressing Variability and Low-Frequency Noise for FinFETs by Amorphous Metal Gate Technology, T. Matsukawa, K. Fukuda, Y. Liu, J. Tsukada, H. Yamauchi, Y. Ishikawa, K. Endo, S. O'uchi, S. Migita, W. Mizubayashi, Y. Morita, H. Ota and M. Masahara, National Institute of Advanced Industrial Science and Technology (AIST)

The effectiveness of amorphous metal gate (MG) in suppressing low-frequency noise (LFN) for FinFETs has been thoroughly investigated. The amorphous TaSiN MGs with various compositions provide flexible Vt tuning as well as small V_t variability, namely AV_t. It was found that the TaSiN-MG FinFETs exhibit drastic reduction of LFN in comparison to poly-crystalline TiN MG. Modelling by 3D-TCAD reveals that work function variation of MG has a significant impact on LFN generation. Suppression of AV_t and LFN is highly beneficial to conduct further scaling of analog/digital components in SoC.

9:30 a.m.
12.2 A Circuit Level Variability Prediction of Basic Logic Gates in Advanced Trigate CMOS Technology, E.R. Hsieh, C.M. Hung, T.Y. Wang, S.S. Chung, R.M. Huang*, C.T. Tsai* and T.R. Yew*, National Chiao Tung University, *United Microelectronics Corporation

Variability has been one of the major scaling issues in advancing the CMOS technology. In this paper, a variation model from the device level to circuit level has been proposed and demonstrated on advanced trigate CMOS. First, a simple and accurate transport model was developed to model variability at the device level. It was then implemented in Spice and the calculation of variation of basic logic gate building block was demonstrated with only *W/L* and the slopes, A_{vt}, A_{gm}, in the Pelgrom plot, as inputs. Finally, a unified simple analytic form was developed to predict the variability of various logic circuits regardless of the number of devices and the arrangement of the circuit.

9:55 a.m.
12.3 Ultra-High-Q Air-Core Slab Inductors for On-Chip Power Conversion, N. Wang, D. Goren, E. O'Sullivan, X. Zhang, W. Gallagher, P. Herget and L. Chang, IBM T. J. Watson Research Center

Air-core slab inductors with specially designed current return paths are proposed to achieve the ultra-high Q required for on-chip power delivery and management at >90% efficiency. Uniquely optimized for buck converter circuits, this CMOS-compatible structure avoids the challenges of thin-film magnetics. Q~25-30 at 200-300MHz is experimentally demonstrated.

10:20 a.m.
12.4 Efficient Wireless Power Transmission Technology Based on an Above CMOS Integrated (ACI) High Quality Inductors, S. Raju, X. Li, Y. Lu, C.-Y. Tsui, W.-H. Ki, M. Chan and C. P. Yue, The Hong Kong University of Science and Technology

A fully-integrated on-chip inductor with 200nH/mm^2 inductance density and a qualify factor of 25 is demonstrated. Utilizing this inductor, a 2.5×2.5mm^2 wireless power harvesting antenna was implemented. It can receive 27mW from a 250mW transmitting power at a 5.3mm distance, which is 7 times more efficient than other reported technologies.

10:45 a.m.
12.5 A Magnetic Tunnel Junction Based True Random Number Generator with Conditional Perturb and Real-Time Output Probability Tracking, W.H. Choi, Y. Lv, J. Kim, A. Deshpande, G. Kang, J.-P. Wang and C.H. Kim, University of Minnesota

This work experimentally demonstrates for the first time a True Random Number Generator (TRNG) based on the random switching probability of Magnetic Tunnel Junctions (MTJs). A conditional perturb and real-time probability tracking scheme is proposed to enhance the reliability, speed, and power consumption while maintaining a 100% bit efficiency.

11:10 a.m.

12.6 DTMOS Mode as an Effective Solution of RTN Suppression for Robust Device/Circuit Co-Design, S. Guo, R. Huang, P. Hao, M. Luo, P. Ren, J. Wang*, W. Bu*, J. Wu*, W. Wong*, S. Yu*, H. Wu*, S.-W. Lee*, Y. Wang and R. Wang, Peking University, *Semiconductor Manufacturing International Corporation

In this paper, using DTMOS as an effective solution of RTN suppression without device/circuit performance penalty is proposed and demonstrated for the first time, with experimental verification and circuit analysis. The experiments show that RTN amplitude is greatly reduced in DTMOS mode, which is even better than the body-biasing technique of FBB, due to the efficient dynamic modulation mechanism. Circuit stability and performance degradation induced by RTN are much improved in the design using DTMOS. New characteristics of RTN physics in DTMOS are also observed and studied in detail. The results are helpful to the robust and reliable device/circuit co-design in future nano-CMOS technology.

11:35 a.m.

12.7 Poly Pitch and Standard Cell Co-Optimization Below 28nm, M. Frederick, ARM INC.

It is well understood that process scaling no longer is following a path of traditional pitch or even device type scaling. With interconnect scaling differently from device and cost scaling as complex functions of different processing options, designing a standard cell platform which achieves optimal power, performance, and density/cost can no longer be achieved by traditional practices. To make matters more complex, rare is the situation where the standard cell or process design team knows in advance the specifics of SoC designs that will later prove to be the majority of the process volume. This paper will explore how poly pitch impacts block level power, performance, and area.