Session 39: Compound Semiconductor and High Speed Devices - High Performance III-V Devices and Technology Towards 5G
Wednesday, December 5, 1:30 PM
Continental Ballroom 6
Co-Chairs: E. Lind, Lund University
Y. Sun, IBM

1:35 PM - 2:00 PM
39.1 First Transistor Demonstration of Thermal Atomic Layer Etching: InGaAs FinFETs with sub-5 nm Fin-width Featuring *in-situ* ALE-ALD, *W. Lu, Y. Lee*, J. Murdzek*, J. Gertsch*, A. Vardi, L. Kong, S. M. George*, and J. A. del Alamo, Massachusetts Institute of Technology, *University of Colorado*

For the first time, thermal atomic layer etching (ALE) on InGaAs-based III-V heterostructures is demonstrated. Also, we report the first transistors fabricated by the thermal ALE technique in any semiconductor system. We further highlight one unique advantage of thermal ALE: its integration with atomic layer deposition in a single vacuum chamber. Using in-situ ALE-ALD, we have fabricated the most aggressively scaled self-aligned In0.53Ga0.47As n-channel FinFETs to date, featuring sub-5 nm fin widths. The narrowest FinFET with Wf = 2.5 nm and Lg = 60 nm shows gm = 0.85 mS/um at Vds = 0.5 V. Devices with Wf = 18 nm and Lg = 60 nm demonstrate gm = 1.9 mS/um at Vds = 0.5 V. Subthreshold swings averaging Slin = 70 mV/dec and Ssat = 74 mV/dec across the entire range of Wf, at minimum Lg = 60 nm have been obtained. These are all record results. The transistors demonstrated here show an average 60% gm improvement over devices fabricated through conventional techniques. These results suggest a very high-quality MOS interface obtained by in-situ ALE-ALD.

2:00 PM - 2:25 PM
39.2 InGaAs-on-Insulator FinFETs with Reduced Off-Current and Record Performance, *C. Convertino, C. Zota, S. Sant*, F. Eltes, M. Sousa, D. Caimi, A. Schenk* and L. Czornomaz, IBM Research Zurich, *Integrated Systems Laboratory, ETH Zurich*

In this work, we demonstrate InGaAs-on-Insulator FinFETs on silicon with optimized on/off trade-off showing record performance. This is achieved by using carefully designed source/drain spacers and spacers extensions to mitigate the off-current, typically high in narrow band-gap materials, as part of a CMOS compatible replacement-metal-gate process flow. Using this technology, devices with LG = 20 nm, spacers width of 10 nm and Wfin = 15 nm achieve record high on-current of 350 µA/µm (IOFF = 100nA/µm and VDD = 0.5 V), for scaled III-V FETs on Si, enabled by an access resistance of 220 Ω µm, SSsat = 78 mV/decade and a gm = 1.5 mS/µm. We analyze the impact of spacers thickness, WFIN and LG on device performance. 2D TCAD simulations provide further insights into device functionality and about the dominant off-state leakage mechanisms.

2:25 PM - 2:50 PM
39.3 Balanced Drive Currents in 10-20 nm Diameter Nanowire All-III-V CMOS on Si, *A. Jönsson, J. Svensson, and L.-E. Wernersson, Lund University*

We use a self-aligned, gate-last process providing n-type (InAs) and p-type (GaSb) MOSFET co-integration with a common gate-stack and demonstrate balanced drive current capability at about 100 µA/µm. By utilizing HSQ-spacers, control of gate-alignment allows to fabricate both n- and p-type devices based on the same type of vertical heterostructure InAs/GaSb nanowire with short gate-lengths down to 60 nm. Refined digital etch techniques, compatible with both sensitive antimonide structures and InAs, enable down to 16 nm diameter GaSb channel regions and 10 nm InAs channels. Balanced performance is

showcased for both n- and p-type MOSFETs with Ion = 156 µA/µm, at Ioff = 100 nA/µm, and 98 µA/µm, at |VDS| = 0.5, respectively.

2:50 PM - 3:15 PM

39.4 High Performance Quantum Well InGaAs-On-Si MOSFETs With sub-20 nm Gate Length For RF Applications, *C. B. Zota, C. Convertino, Y. Baumgartner, M. Sousa, D. Caimi and L. Czornomaz, IBM Research GmbH Zürich Laboratory*

We demonstrate RF-compatible quantum well InGaAs MOSFETs integrated on Si substrates, with LG down to 14 nm and a Si CMOS compatible RMG fabrication flow. Devices exhibit simultaneously extrapolated ft and fmax of 370 and 310 GHz, respectively, the highest reported combined ft/fmax for III-V MOSFETs on Si.

3:15 PM - 3:40 PM

39.5 High Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template Assisted Selective Epitaxy, *S. Lee, C. -W. Cheng, X. Sun, C. D'Emic, H. Miyazoe, M. M. Frank, M. Lofaro, J. Bruley, P. Hashemi, J. A. Ott, T. Ando, W. Spratt, G. M. Cohen, C. Lavoie, R. Bruce, J. Patel, H. Schmid*, L. Czornomaz*, V. Narayanan, R. T. Mo, and E. Leobandung, IBM T. J. Watson Research Center, *IBM Research GmbH Zürich Laboratory*

We report InGaAs gate-all-around nanosheet NFETs on Si substrate using template-assisted-selective-epitaxy (TASE) and a gate-last process with thermal budget advantages. Compared to our early report of the TASE process, in this paper we demonstrate that TASE can be scaled to a channel thickness of ~10 nm, which enables short gate devices without significant leakage. The defects and composition of the fabricated nanosheet FETs are also investigated. Enabled by this VLSI compatible process and a novel high-pressure deuterium annealing process, our 39 nm-Lg device shows a peak gm of 1.37 mS/um, a subthreshold slope in saturation of 72 mV/decade, and an Ion of 355 uA/um at 0.5 V Vgs, the highest among reported sub-50 nm-Lg III-V FETs on Si.

3:40 PM - 4:05 PM

39.6 Scaling Acoustic Filters Towards 5G, *Y. Yang, R. Lu, and S. Gong, University of Illinois at Urbana Champaign*

This paper presents a micro-electro-mechanical system (MEMS) filter at 10.8 GHz as the first step of scaling electromechanical filters towards fifth-generation (5G) frequencies beyond 6 GHz. The scaling of the center frequency to 10. 8 GHz is made possible by resorting to a higher order asymmetrical lamb wave mode (A3) in lithium niobate (LiNbO3) thin film. The filter is then designed as a ladder configuration of A3 resonator arrays to reduce insertion loss and attain a low system impedance. The fabricated resonator has demonstrated an electromechanical coupling (kt2) of 3.6% and a quality factor (Q) of 337. The Q is among the highest reported for piezoelectric MEMS resonators operating at this frequency range. The fabricated filter at 10.8 GHz has a 3 dB bandwidth of 70 MHz, a minimum insertion loss of 3.7 dB, an in-band ripple less than 0.1 dB, and a compact footprint of 0.7x0.5 mm2.