Session 34: Characterization, Reliability, and Yield - Advanced Technology Reliability
Wednesday, December 5, 9:00 AM
Plaza B
Co-Chairs: G. Reimbold, CEA-Leti
B. Weir, Broadcom, Inc.

9:05 AM - 9:30 AM
34.1 Understanding the intrinsic reliability behavior of n-/p-Si and p-Ge nanowire FETs utilizing degradation maps, *A. Chasin, E. Bury, J. Franco, B. Kaczer, M. Vandemaele, H. Arimura, E. Capogreco, L. Witters, R. Ritzenthaler, H. Mertens, N. Horiguchi, D. Linten, imec*

We compare and model the main reliability limitations of stacked Gate-All-Around (GAA) n-/p-channel Silicon and strained p-channel Germanium Nanowire (NW) transistors. Stress measurements in the entire {VG,VD} space allow to separate the different degradation modes and how they interact with each other. We show that these degradation modes are not universal, as they have a different relative weight depending on the considered technology, and that they can show different acceleration mechanisms. Moreover, we also discuss the impact of self-heating effects (SHE) by means of activation energy extraction in the entire {VG,VD} map.

9:30 AM - 9:55 AM
34.2 BTI Reliability Improvement Strategies in Low Thermal Budget Gate Stacks for 3D Sequential Integration, *J. Franco, Z. Wu, G. Rzepa*, A. Vandooren, H. Arimura, L.-Å Ragnarsson, G. Hellings, S. Brus, D. Cott, V. De Heyn, G. Groeseneken, N. Horiguchi, J. Ryckaert, N. Collaert, D. Linten, T. Grasser*, B. Kaczer, imec, *TU Wien*

Low thermal budget gate-stacks will be required for novel integration schemes, such as 3D Sequential stacking of device tiers. We demonstrate two strategies to tolerate the inherently larger high-k defect densities: i) replacing inversion mode devices with highly doped junction-less transistors, or ii) engineering dipoles at the SiO2/HfO2 interface to minimize the carrier-defect interaction. The latter approach is demonstrated for nMOS PBTI and, for the first time, also for pMOS NBTI.

9:55 AM - 10:20 AM
34.3 Characterization and understanding of slow traps in GeO_x-based n-Ge MOS interfaces, *M. Ke, P. Cheng, K. Kato, M. Takenaka, and S. Takagi, The University of Tokyo*

The properties of slow electron traps in n-Ge MOS interfaces over a wide range of electrical field across gate oxides (Eox) are systematically investigated. It is found through careful examination of the C-V hysteresis that slow trapping under low Eox conditions is attributed only to electron trapping into existing slow traps. Under large Eox conditions, on the other hand, generation of slow electron traps and hole trapping are found to additionally affect the slow trapping characteristics. We propose a new measurement scheme to discriminate existing and generated slow electron traps and apply this method to the three different GeOx-based MOS interfaces in order to clarify the nature of slow traps. It is revealed from this analysis that a pre-plasma oxidation process reduces existing slow electron traps and improves slow trapping in low Eox. On the other hand, ultrathin Y2O3 insertion reduces generation of slow electron traps and improves slow trapping in high Eox.

10:20 AM - 10:45 AM
34.4 Soft Error Trends in Advanced Silicon Technology Nodes (Invited), *B. Bhuva, Vanderbilt University*

Soft errors for planar and FinFET nodes have shown different trends for various designer-controlled parameters. This paper examines effects of some of these parameters for the 20-nm Planar and the 16-nm FinFET technology nodes. Latchup vulnerability of FinFET node is also investigated through simulations.

10:45 AM - 11:10 AM

34.5 CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI, *J. Jiang, J. H. Chu, and K. Banerjee, University of California, Santa Barbara*

Cu interconnects suffer from steep rise in resistivity and severe reliability degradation for sub-20 nm line widths. Other metals, including Co and Ru, have been demonstrated with higher electromigration (EM) resistance, but exhibit lower electrical conductivity that degrades circuit performance. This work reports multilayer graphene (MLG) directly grown on SiO2 substrate at 300 °C by a novel pressure-assisted solid-phase diffusion synthesis method, and, for the first time, demonstrates a CMOS-compatible intercalation doped graphene nanoribbon (DGNR) interconnect technology with smaller electrical resistivity than Cu, Co and Ru interconnects. The DGNR interconnect also exhibits < 4% conductivity degradation over 1000 hours at room temperature (RT) without any encapsulation or barrier layer, and negligible EM under 100 MA/cm2 current stress test at > 100 °C. The high current carrying capability of DGNR allows more aggressive vertical scaling w.r.t Cu, Co, or Ru, leading to lower parasitics and significantly smaller switching energy.

11:10 AM - 11:35 AM

34.6 Time Dependent Early Breakdown of AlGaN/GaN Epi Stacks and Shift in SOA Boundary of HEMTs Under Fast Cyclic Transient Stress, *B. Shankar, A. Soni, S. D. Gupta, S. Shikha, S. Singh, S. Raghavan and M. Shrivastava, Indian Institute of Science*

This experimental study reports first observations of (i) SOA boundary shift in GaN HEMTs and (ii) early time to fail of vertical AlGaN/GaN Epi stack under fast changing (sub-10ns risetime) cyclic transient stress conditions for a 600V qualified commercial grade HEMT stack. It is shown that a stack qualified for 10 years lifetime under DC stress, fails faster under cyclic transient stress. Integrated electrical and mechanical stress characterization routine involving Raman/PL mapping and CL spectroscopy reveals material limited unique failure physics under transient stress condition. Failure analysis using cross-sectional TEM investigations reveal signature of different degradation and failure mechanism under transient and DC stress conditions. A failure model is proposed for failure under cyclic transient stress.