Session 31: Nano Device Technology - NCFET Physics and Devices
Wednesday, December 5, 9:00 AM
Continental Ballroom 5
Co-Chairs: K.-L. Cheng, TSMC
T. Yamashita, Renesas Electronics

9:05 AM - 9:30 AM
31.1 New Insights into the Physical Origin of Negative Capacitance and Hysteresis in NCFETs, *H. Wang, M. Yang, Q. Huang, K. Zhu, Y. Zhao, Z. Liang, C. Chen, Z. Wang, Y. Zhong, X. Zhang, R. Huang, Peking University*

In this paper, direct experimental observation of negative capacitance (NC) in a standalone ferroelectric (FE) capacitor is reported for the first time, which proves that the physical origin of NC is the domain switching dynamics rather than the stabilized switching. Based on this origin, the "dynamic polarization (DP) matching", different from the traditional capacitance matching, is rigorously derived and verified to be the prerequisite for sub-60mV/dec subthreshold swing (SS) in NCFET. The proposed DP matching can accurately describe and predict the features of NCFET based on our developed device model, showing that the SS and hysteresis are highly sensitive to the input sweeping voltage and FE switching dynamics, as well as other device parameters. Moreover, an intrinsic conflict is found between hysteresis and SS optimization. This work provides new understanding for the NCFET mechanism.

9:30 AM - 9:55 AM
31.2 A Critical Examination of 'Quasi-Static Negative Capacitance' (QSNC) theory, *Z. Liu, A. Bhuiyan, and T. P. Ma, Yale University*

Recent years have seen a boom in the interest of using the alleged ferroelectric 'negative capacitance' to realize low subthreshold swing of MOSFETs. According to the "quasistatic negative capacitance' (QSNC) theory, a ferroelectric (FE) capacitor has an intrinsic but unstable 'negative capacitance' (NC) region. By adding a matching linear dielectric (DE) capacitor in series, it is possible to 'stabilize' the NC region. In this work, we examined the validity of the QSNC theory, and performed several key experiments to verify that experimental results are consistent with our theoretical assessment. Unfortunately, our overall results do not support the QSNC theory.

9:55 AM - 10:20 AM
31.3 Direct relationship between sub-60 mV/dec subthreshold swing and internal potential instability in MOSFET externally connected to ferroelectric capacitor, *X. Li, A. Toriumi, The University of Tokyo*

Negative-capacitance effect on subthreshold-swing (SS) improvement in ferroelectric-FETs is still under debate. We demonstrate the direct correlation between sub-60 mV/dec SS and internal-potential enhancement in MOSFET externally connected to ferroelectric-capacitor. The results support that reported steep SS are tightly related to ferroelectric domain switching rather than the ideal negative-capacitance effect.

10:20 AM - 10:45 AM
31.4 Assessment of Steep-Subthreshold Swing Behaviors in Ferroelectric-Gate Field-Effect Transistors Caused by Positive Feedback of Polarization Reversal, *S. Migita, H. Ota, and A. Toriumi*, National Institute of Advanced Industrial Science and Technology (AIST), *The University of Tokyo*

Steep-subthreshold swing (SS) behaviors in ferroelectric-gate field-effect transistors (Fe-FETs) are investigated using the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gates stack structures

with different area ratios between MIS and MFM capacitors. It is analyzed that the capacitance matching between them by adjusting the area ratio is significant to efficiently utilize the polarization reversal behavior in the ferroelectric layer. In this work we explain the steep-SS behavior from viewpoint of positive feedback of polarization reversal. Furthermore it is discussed why steep-SS is observable in recent Fe-FETs.

10:45 AM - 11:10 AM

31.5 Experimental Study on The Role of Polarization Switching in Subthreshold Characteristics of HfO_2-based Ferroelectric and Anti-ferroelectric FET, *C. Jin, K. Jang, T. Saraya, T. Hiramoto, and M. Kobayashi, The University of Tokyo*

We have experimentally studied and revealed the direct relationship between polarization switching and steep subthreshold slope (SS) characteristics of HfO2-based ferroelectric FET (FeFET) and Anti-FeFET (A-FeFET) by systematically designing and fabricating devices, and monitoring Ig with high resolution, for the first time. In the circumstances that charge injection prevents polarization switching from occurring in subthreshold region of FeFET, we have obtained two major findings: (1) Sub-60 SS as low as 23.5 mV/dec is observed by adjusting Vg bias sequence, which is attributed to charge injection assisted by polarization switching. (2) Anti-ferroelectric facilitates to align polarization switching in subthreshold region and SS can be improved in A-FeFET as a consequence, which is directly observed by monitoring I_g.

11:10 AM - 11:35 AM

31.6 Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$, *M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, NaMLab gGmbH*

We report the experimental observation of hysteresis-free negative capacitance (NC) in thin ferroelectric Hf0.5Zr0.5O2 (HZO) films through high-speed pulsed charge-voltage measurements. Hysteretic switching is suppressed by the addition of thin Al2O3 layers on top of the HZO to prevent the screening of the polarization. We observe an S-shaped polarization-electric field dependence without hysteresis in agreement with Landau theory, which enables direct extraction of NC modeling parameters for ferroelectric HZO. Hysteresis-free NC is demonstrated down to 100 ns pulse widths limited only by our measurement setup. These results give critical insights into the physics of ferroelectric NC and practical NC device design using ferroelectric HZO.

11:35 AM - 12:00 PM

31.7 Negative-Capacitance FinFET Inverter, Ring Oscillator, SRAM Cell, and Ft, *K.-S. Li, Y.-J. Wei, Y.-J. Chen, W.-C. Chiu, H.-C. Chen, M.-H. Lee*, Y.-F. Chiu, F.-K. Hsueh, B.-W.Wu, P.-G. Chen, T.-Y. Lai, C.-C. Chen, J.-M. Shieh, W.-K. Yeh, S. Salahuddin***, C. Hu**, National Applied Research Laboratories, *National Taiwan Normal University, **National Chiao Tung University, ***University of California, Berkeley*

In this work, we use thermal-ALD to prepare ferroelectric HfZrO2 (HZO) thin film with thickness from 3 to 7 nm for the NC-FinFET's gate stack. The subthreshold swing (SS) was as low as 5 mV/dec (SSmin) over 4 orders of ID. Lower thermal budget process, CO2 far-infrared laser activation and 400 oC Ni silicide were employed in the 2-level metal backend integration for maintaining orthorhombic phase in HZO thin film and minimizing the hysteresis in IV. NC-FinFET inverter has 77% higher voltage gain compared to FinFET-inverter employing HfO2 gate dielectric. NC-FinFET ring oscillator exhibited small speed and power advantages over FinFET oscillator. For the first time, NC-FET cut-off frequency (Ft) frequency is measured, 23.08 GHz for NC-FniFET versus 18.85 GHz for the control FinFET and NC-FinFET SRAM was observed to exhibit excellent noise margin.

12:00 PM - 12:25 PM

31.8 Extremely Steep Switch of Negative-Capacitance Nanosheet GAA-FETs and FinFETs, *M. H. Lee, K.-T. Chen, C.-Y. Liao, S.-S. Gu, G.-Y. Siang, Y.-C. Chou, H.-Y. Chen, J. Le, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, P.-G. Chen*, M. Tang**, Y.-D. Lin***, H.-Y. Lee***, K.-S. Li*, and C. W. Liu+, National Taiwan Normal University, *National Nano Device Laboratories, ** PTEK Technology Co., Ltd, ***Industrial Technology Research Institute, +National Taiwan University*

Extremely steep switch of NC Nanosheet (NS) GAA-FETs and FinFETs are experimentally presented with SSavg/SSmin=22/14mV/dec and SSavg/SSmin=38/21mV/dec, respectively. The sub-60mV/dec current magnitude of sub-60mV/dec is >4 and ~5 decades for NC-NSGAA and NC-FinFET, respectively, as well as apparent N-DIBL and NDR. The SS depends on WFin/L ratio, and WFin < L is the solution to achieve sub-60mV/dec. The uniform size of each NS for stacked NC-NSGAA is an important issue to optimize the NC effect with SS=19mV/dec.