Session 27: Memory Technology - MRAM & PCRAM
Wednesday, December 5, 9:00 AM
Grand Ballroom A
Co-Chairs: S. Kang, Qualcomm Technology Inc.
G. Navarro, CEA-Leti

9:05 AM - 9:30 AM
27.1 22-nm FD-SOI Embedded MRAM Technology for Low-Power Automotive-Grade-1 MCU Applications, *K. Lee, R. Chao, K. Yamane, V. B. Naik, H. Yang, J. Kwon, N. L. Chung, S. H. Jang, B. Behin-Aein, J. H. Lim, S. K, B. Liu, E. H. Toh, K. W. Gan, D. Zeng, N. Thiyagarajah, L. C. Goh, T. Ling, J. W. Ting, J. Hwang, L. Zhang, R. Low, R. Krishnan, L. Zhang, S. L Tan, Y. S. You, C. S. Seet, H. Cong, J. Wong, S. T. Woo, E. Quek, S. Y. Siah, GLOBALFOUNDRIES*

We demonstrate 22-nm FD-SOI 40Mb embedded MRAM (eMRAM) macros for automotive-grade-1 (Auto-G1) MCU applications, highlighting sub-ppm t0 bit error rate and zero failure after 1M endurance cycles across Auto-G1 operating temperature range (-40~150 °C). Read disturbance characterization with external field also reveals that 40Mb eMRAM macro is capable of active-mode magnetic immunity > 500 Oe at 150 °C. In addition, based on 22-nm eMRAM macro data, we review the effects of magnetic tunnel junction (MTJ) size on reliability and examine scalability of eMRAM technology beyond 22 nm.

9:30 AM - 9:55 AM
27.2 14ns write speed 128Mb density Embedded STT-MRAM with endurance>10^{10} and 10yrs retention @85°C using novel low damage MTJ integration process, *H. Sato, H. Honjo, T. Watanabe, M. Niwa, H. Koike, S. Miura, T. Saito, H. Inoue, T. Nasuno, T. Tanigawa, Y. Noguchi, T. Yoshiduka, M. Yasuhira, S. Ikeda, S.- Y. Kang*, T. Kubo*, K. Yamashita*, Y. Yagi*, R. Tamura**, and T. Endoh, Tohoku University, *Tokyo Electron Ltd., **Advantest Corp.*

By developed novel damage-control-integration-process technology with new low-damage unit PVD/RIE/SiN-cap process, TMR, thermal stability, and switching efficiency improved by a factor of 1.7, 9, and 9, respectively, and its endurance is over 10^10, although thermal stability drastically increased. Finally, 14ns-write speed at 1.2V-Vdd was successfully demonstrated using our 128Mb-density-STT-MRAM.

9:55 AM - 10:20 AM
27.3 STT-MRAM devices with low damping and moment optimized for LLC applications at 0x nodes, *L. Thomas, G. Jan, S. Serrano-Guisan, H. Liu, J. Zhu, Y.-J. Lee, S. Le, J. Iwata-Harms, R.-Y. Tong, S. Patel, V. Sundar, D. Shen, Y. Yang, R. He, J. Haq, Z. Teng, V. Lam, P. Liu, Y.-J. Wang, T. Zhong, H. Fukuzawa, and P.K. Wang, TDK- Headway Technologies, Inc.*

Last-Level-Cache applications at 0X technology nodes require devices switching reliably in less than 10ns at currents smaller than 50uA, while preserving data retention up to 85°C. In this paper, we show that both low Gilbert damping and low magnetic moment are the primary factors for efficient writing at nanosecond time scales. We report comprehensive device-level measurements of damping using both conventional free layer designs and an optimized free layer that combines low damping and low moment and meets LLC requirements.

10:20 AM - 10:45 AM
27.4 Microwave neural processing and broadcasting with spintronic nano-oscillators (Invited), *P. Talatchian, M. Romera, S. Tsunegi*, F. Abreu Araujo, V. Cros, P. Bortolotti, J. Trastoy, K. Yakushiji*, A. Fukushima*, H. Kubota*, S. Yuasa*, M. Ernoult, D. Vodenicarevic, T. Hirtzlin, N. Locatelli, D. Querlioz,*

*J. Grollier, Thales, Univ. Paris-Sud, Université Paris-Saclay, *National Institute of Advanced Industrial Science and Technology (AIST)*

Can we build small neuromorphic chips capable of training deep networks with billions of parameters? This challenge requires hardware neurons and synapses with nanometric dimensions, which can be individually tuned, and densely connected. While nanosynaptic devices have been pursued actively in recent years, much less has been done on nanoscale artificial neurons. In this paper, we show that spintronic nano-oscillators are promising to implement analog hardware neurons that can be densely interconnected through electromagnetic signals. We show how spintronic oscillators maps the requirements of artificial neurons. We then show experimentally how an ensemble of four coupled oscillators can learn to classify all twelve American vowels, realizing the most complicated tasks performed by nanoscale neurons.

10:45 AM - 11:10 AM

27.5 High Endurance Phase Change Memory Chip Implemented based on Carbon-doped $Ge_2Sb_2Te_5$ in 40 nm Node for Embedded Application, *Z. T. Song, D. L. Cai, X. Li, L. Wang*, Y. F. Chen, H. P. Chen, Q. Wang, Y. P. Zhan*, M. H. Ji*, Chinese Academy of Sciences, *Semiconductor Manufacturing International Corporation*

We present the results of a highly reliable PCM based on Carbon-doped Ge2Sb2Te5 material in 40 nm node. The chip exhibits excellent data retention, endurance characteristics, and the sensing window is even larger after 260 °C soldering test. PCM is suitable for applications requiring high thermal stability and cycling endurance.

11:10 AM - 11:35 AM

27.6 A 40nm Low-Power Logic Compatible Phase Change Memory Technology, *J.Y. Wu, Y.S. Chen, W.S. Khwa, S.M. Yu, T.Y. Wang, J.C. Tseng, Y.D. Chih and Carlos H. Diaz, Taiwan Semiconductor Manufacturing Company Ltd.*

An embedded phase change memory technology in 40nm low-power logic platform is demonstrated with minimal added process complexity - two non-critical additional masks over standard logic. Specially designed hard mask and etching process was used to achieve 50% shrinkage of the memory cell bottom electrode dimension with same lithography tooling as the 40nm logic platform. Bottom electrode CD shrinkage along with optimization of the electrode materials in terms of electrical and thermal conductivity enabled significant (~4x) write current reduction attaining competitive levels of ~300 μA at 40nm BE CD. Embedded PCM cells reported in this work demonstrated over 100x memory window - (RESET/SET resistance switching ratio), over 200k cycling endurance with extrapolated 10 year retention at 120 °C. In this work not only large switching resistance ratios but also highly-controllable resistance values that are almost independent of the PCM starting resistance state are presented along with the corresponding programing pulse requirements. The switching resistance ratio and resistance value controllability are key features for neural network and compute-in-memory applications. In this work, their benefits on design margins for energy efficient high-density binary neural network for inference applications aiming accuracy levels of well over 90% is asserted over an MNIST dataset.

11:35 AM - 12:00 PM

27.7 8-bit Precision In-Memory Multiplication with Projected Phase-Change Memory, *I. Giannopoulos*, A. Sebastian*, M. Le Gallo, V.P. Jonnalagadda, M. Sousa, M.N. Boon, and E. Eleftheriou, IBM Research – Zurich*

In-memory computing is an emerging non-von Neumann approach in which certain computational tasks such as matrix-vector multiplication are performed using resistive memory devices organized in a crossbar array. However, the conductance variations associated with the memory devices limit the precision of this

computation. Here, we demonstrate that the so-called projected phase-change memory (Proj-PCM) devices can achieve 8-bit precision while performing scalar multiplication. The devices were fabricated and characterized using electrical measurements and STEM investigation. They are found to be remarkably immune to conductance variations arising from structural relaxation, 1/f noise and temperature variations. Moreover, it is possible to compensate for the temperature-dependent conductance variations in a crossbar array using a simple model. Finally, we experimentally demonstrate a neural network-based image classification task involving 30 such Proj-PCM devices.