**Session 7: Process and Manufacturing Technology - 3D Integration and Memory Technologies**
Monday, December 3, 1:30 PM
Continental Ballroom 6
*Co- Chairs: P. Baars, GLOBALFOUNDRIES*
*T. Ando, IBM*

1:35 PM - 2:00 PM
**7.1 First Demonstration of 3D stacked Finfets at a 45nm fin pitch and 110nm gate pitch technology on 300mm wafers.,** *A. Vandooren, J. Franco, Z. Wu*, B. Parvai**, W. Li, L. Witters, A. Walke, L. Peng, V. Deshpande, N. Rassoul, G. Hellings,G. Jamieson, F. Inoue, K. Devriendt, L. Teugels, N. Heylen, E. Vecchio, T. Zheng, E. Rosseel, W. Vanherle, A. Hikavyy, G. Mannaert, B. T. Chan, R. Ritzenthaler, J. Mitard, L. Ragnarsson, N. Waldron, V. De Heyn, S. Demuynck, J. Boemmels, D. Mocuta, J. Ryckaert and N. Collaert, imec, *also with KULeuven, Leuven, Belgium, **also with VUB, Brussels, Belgium*

3D stacking using a sequential integration approach is demonstrated for finfet devices on 300mm wafers at a 45nm fin pitch and 110nm poly pitch technology. This demonstrates the compatibility of the 3D sequential approach for aggressive device density stacking at advanced nodes thanks to the tight alignment precision of the first processed top layer to the last processed bottom layer through the top silicon channel and bonding stack during 193nm immersion lithography. The top devices are junction-less devices fabricated at low temperature (T≤525°C) in a top Si layer transferred by wafer-to-wafer bonding with a bonding dielectric stack down to 170nm. The top devices offer similar performance as the high temperature bulk finfet technology for LSTP applications. The use of TiN/TiAl/TiN/HfO2 gate stack provides the proper threshold voltage adjustment while the insertion of the LaSiOx dipole improves device performance and brings the BTI reliability within specification at low temperature.

2:00 PM - 2:25 PM
**7.2 Breakthroughs in 3D Sequential Technology,** *L. Brunet, C. Fenouillet-Beranger, P. Batude, S. Beaurepaire, F. Ponthenier,2, N. Rambal,2, V. Mazzocchi, J-B. Pin**, P. Acosta-Alba, S. Kerdiles, P. Besson*, H. Fontaine, T. Lardin, F. Fournel, V. Larrey, F. Mazen, V. Balan, C. Morales, C. Guerin, V. Jousseaume, X. Federspiel*, D. Ney*, X. Garros, A. Roman,2, D. Scevola,2, P. Perreau, F. Kouemeni-Tchouake, L. Arnaud, C. Scibetta, S. Chevalliez, F. Aussenac, J. Aubin***, S. Reboh, F. Andrieu, S. Maitrejean, M. Vinet, CEA-LETI, *STMicroelectronics, **Applied Materials Inc., *** SCREEN LASSE*

In this paper, we present technological levers to bring 3D sequential integration compatible with industrial requirements. First, in term of low temperature challenges, low resistance gate stack have been achieved using nanosecond laser and results of a full 500°C raised source & drain (RSD) epitaxy are also presented. Then, integration of intermediate Back End Of Lines (iBEOL) levels is studied from the contamination management to the thermal stability in terms of reliability and low-k morphology. Finally, a Smart CutTM process above a CMOS wafer is presented for the first time.

2:25 PM - 2:50 PM
**7.3 Hybrid bonding for 3D stacked image sensors: impact of pitch shrinkage on interconnect robustness,** *J. Jourdon,, S. Lhostis, S. Moreau**, J. Chossat, M. Arnoux***, C. Sart, Y. Henrion, P. Lamontagne, L. Arnaud**, N. Bresson**, V. Balan**, C. Euvrard**, Y. Exbrayat**, D. Scevola, E. Deloffre, S. Mermoz, A. Martin***, H. Bilgen, F. Andre, C. Charles, D. Bouchu**, A. Farcy, S. Guillaumet, A. Jouve**, H. Fremont*, and S. Cheramy**, STMicroelectronics, *University of Bordeaux, **CEA-LETI, ***STMicroelectronics*

We present the first 3D-stacked CMOS Image Sensor with a bonding pitch of 1.44 μm. The influence of the hybrid bonding pitch shrinkage (8.8 to 1.44 μm) from the process point of view to a functional device via the robustness aspect is studied. Smaller bonding pads do not lead to any specific failure

2:50 PM - 3:15 PM

**7.4 Embedded Select in Trench Memory (eSTM), best in class 40nm floating gate based cell: a process integration challenge (Invited),** *S. Niel, F. La Rosa, A. Regnier , M. Mantelli, F. Trenteseaux, G. Ghezzi, A. Marzaki, Q. Hubert, J. Delalleau, T. Cabout ,F. Maugain, E. Lepape, L. Baron, A. Champenois, D. Galpin, N. Cherault, S. Audran, L. Parmigiani, P. Gouraud, B. Duclaux, Y. Escarabajal, F. Baudin, E. Beche, B. Saidi, V. Arnal, STMicroelectronics*

This paper discusses an innovative architecture of charge storage NVM cell, which outpaces state-of-the-art in term of bit-cell area. This new concept of memory cell is used today in production for microcontrollers. After cell architecture and activation description, we will present process flow integration challenges, process optimizations and single cell characterizations.

*3:15 PM Coffee Break*

3:40 PM - 4:05 PM

**7.5 Highly Reliable Ferroelectric Hf0.5Zr0.5O2 Film with Al Nanoclusters Embedded by Novel Sub-Monolayer Doping Technique,** *T. Yamaguchi, T. Zhang, K. Omori, Y. Shimada*, Y. Kunimune*, T. Ide*, M. Inoue, and M. Matsuura, Renesas Electronics Corp., Renesas Electronics Corporation, *Renesas Semiconductor Manufacturing Co.*

Highly reliable ferroelectric (FE) Hf0.5Zr0.5O2 (HZO) film with Al nanoclusters embedded by sub-monolayer doping technique is demonstrated for the first time. Al nanoclusters increase the remnant polarization (Pr) and reduce the voltage necessary for polarization switching. Furthermore, the program and erase endurance at the cycle of more than 250k and the Pr retention at 85ºC for 10 years are achieved. Al nanoclusters are formed by the partial oxidation of sub-monolayer metallic Al embedded in HZO films. Al nanoclusters enhance the large grain growth of the orthorhombic-phase HZO during FE-HZO crystallization annealing. The reduction of grain boundaries caused by the large grain growth with Al nanoclusters effectively reduces the leakage current. As a result, the reliability of the FE HZO film is significantly improved.

4:05 PM - 4:30 PM

**7.6 Interface Dipole Modulation Memory based on Multi-stacked HfO2/SiO2 MOS Structure,** *N. Miyata, J. Nara*, T. Yamasaki*, K. Sumita, R. Sano**, and H. Nohira**, AIST, *NIMS, **Tokyo City University*

We report an interface dipole modulation (IDM) in HfO2-based MOS stack structures. Experimental evidence for IDM was exhibited, and rearrangement of interfacial Ti-O configuration was theoretically demonstrated to cause IDM. Multi-stack HfO2/SiO2 IDM structures are promising in terms of a low temperature process, practical memory window, and stable potential switching.

4:30 PM - 4:55 PM

**7.7 Ge-based Non-Volatile Logic-Memory Hybrid Devices for NAND Memory Application,** *N. Wei, B. Chen, Z. Zheng, Z. Cai, R. Zhang, R. Cheng, S-W Lee, Y. Zhao, Zhejiang University*

In this work, novel Ge-on-Insulator (GeOI) MOSFETs with resistive-switchable gate stacks, named RFETs, are proposed and experimentally realized. The junctionless GeOI RFET and typical inversion-mode GeOI RFET are fabricated and both types of RFETs exhibit decent transistor behaviors and RRAM characteristics at the same time. Furthermore, by utilizing these two types of RFETs, a new GeOI RFET-based NAND memory is constructed and the memory functions of the arrays are experimentally demonstrated. This RFET-based NAND memory has a simple cell structure and very simplified I/O circuit in comparison with

the conventional flash memory and non-volatile memory such as RRAM and MRAM. Therefore, RFETs should be promising for the applications of next-generation high density, low power memory and in-memory computing and neuromorphic computing.