Session 2: Memory Technology - Charge Based Memories
Monday, December 3, 1:30 PM
Grand Ballroom A
Co- Chairs: M. Kobayashi, The University of Tokyo
J. Lee, Samsung Electronics

1:35 PM – 2:00 PM
2.1 Scaling Trends in NAND Flash (Invited), *K. Parat and A. Goda*, Intel Corporation, *Micron Technology*

As the 2D NAND Flash scaling plateaued, 3D NAND Flash emerged as a strong successor to continue the scaling trend. Improved cell characteristics of 3D NAND have enabled 4bits/cell capability, allowing for additional scaling. This paper describes recent innovations in 3D NAND technology and key challenges ahead for continued scaling.

2:00 PM - 2:25 PM
2.2 Analysis and Realization of TLC or even QLC Operation with a High Performance Multi-times Verify Scheme in 3D NAND Flash memory, *C.C. Lu, C.C. Cheng, H.P. Chiu, W.L. Lin,T.W. Chen, S.H. Ku, Wen-Jer Tsai, T.C. Lu*, K.C. Chen, Tahui Wang*, C.-Y. Lu*, *Macronix International Co., Ltd., *National Chiao-Tung University*

Feasibility of multi-times verify (MTV) scheme on triple-level cell (TLC) and quad-level cell (QLC) operations of charge-trap storage 3D NAND memories is investigated comprehensively. Results reveal that random telegraph noise (RTN) and program noise are the major factors affecting lower (LB) and upper boundaries (HB) of Vt distribution, respectively. Enlargement of operation window and reduction of ECC usage with MTV scheme to mitigate RTN-induced LB tail are demonstrated on TLC and QLC operations. In addition, the impact of program noise on HB Vt under various process conditions and ISPP steps is studied experimentally and also explained by our Monte Carlo simulator. Finally, program performance and reserved margin with and without MTV scheme applied on TLC and QLC operation are demonstrated.

2:25 PM - 2:50 PM
2.3 Implementing Spike-Timing-Dependent Plasticity and Unsupervised Learning in a Mainstream NOR Flash Memory Array, *G. Malavena, A. S. Spinelli, and C. Monzio Compagnoni, Politecnico di Milano*

In this work, we present the first implementation of spike-timing-dependent plasticity (STDP) and unsupervised learning in a mainstream NOR Flash memory array based on floating-gate cells. A simple yet effective word-line and bit-line pulse scheme is proposed to make a common-ground double-polysilicon NOR array in 40 nm embedded technology work as an artificial synaptic array in a spiking neural network learning according to the STDP rule, with no change required either to the array or to the cell design. With this scheme, long-term potentiation and long-term depression of the synaptic weights are achieved, respectively, by hot-hole injection and channel hot-electron injection at the drain side of the cells. Unsupervised learning is experimentally demonstrated in the array, paving the way for the development of large-scale and high-density neuromorphic systems based on mainstream nonvolatile memory technologies.

2:50 PM Coffee Break

3:15 PM - 3:40 PM
2.4 A Novel Voltage-Accumulation Vector-Matrix Multiplication Architecture Using Resistor-shunted Floating Gate Flash Memory Device for Low-power and High-density Neural Network Applications, *Y.-Y. Lin, F.-M. Lee, M.-H. Lee, W.-C. Chen, H.-L. Lung, K.-C. Wang, and C.-Y. Lu,*

Macronix International Co., Ltd.

We propose a novel processing-in-memory (PIM) architecture based on the voltage summation concept to accelerate the vector-matrix multiplication for neural network (NN) applications. The core device is formed by adding a buried shunt resistor to a floating gate Flash memory device. The NN string is constructed the same way as in NAND Flash by connecting the core devices in series. In perceptron operation the weighting factors are stored in the floating gate device and the sum-of-product is readily obtained by summing the voltage drop of the cells in each NN string. The energy consumption for 128 multiply-and-sum operations within a string can be as low as 0.2pJ. Finally, with the weight values stored in the non-volatile memory there is no need to move data around and this greatly improves the performance and energy efficiency for neural network applications.

3:40 PM - 4:05 PM
2.5 Vertical Ferroelectric HfO2 FET based on 3-D NAND Architecture: Towards Dense Low-Power Memory, *K. Florent, M. Pesic*, A. Subirats, K. Banerjee, S. Lavizzari, A. Arreghini, L. Di Piazza, G. Potoms, F. Sebaai, S. R. C. McMitchell, M. Popovici, G. Groeseneken, and J. Van Houdt,*
*imec, also with ESAT- KU Leuven, *MDLSoft Inc.*

A vertical ferroelectric HfO2 field effect transistor based on 3-D macaroni NAND architecture is reported for the first time. Up to 2 V memory window was obtained after the application of 100 ns program/erase pulses. Flash-like endurance of 1E4 cycles is reported and first reliability assessments were performed.

4:05 PM - 4:30 PM
2.6 Hybrid 1T e-DRAM and e-NVM Realized in One 10 nm node Ferro FinFET device with Charge Trapping and Domain Switching Effects, Q. Luo, T. Gong, Y. Cheng**, *Q. Zhang, H. Yu, J. Yu, H. Ma, X. Xu, K. Huang, X. Zhu, D. Dong, J. Yin, P. Yuan, L. Tai, J. Gao, J. F. Li, H. Yin, S. Long, Q. Liu, H. Lv, M. Liu, Chinese Academy of Sciences, *University of the Chinese Academy of Sciences, **East China Normal University*

For the first time, we experimentally demonstrated a 10 nm node HfZrO based FE-FinFET device with both Charge Trapping and Domain Switching memory effect. Extreme high endurance ($>10^{12}$), high operation speed (< 20ns), good data retention (104@85°C), low operation voltage (<3 V) were identified in charge trapping mode, which is quite promising for e-DRAM application. As the device working in domain switching mode, even more robust retention (>10 years) and read disturbance immunity were achieved, showing great potential for e-NVM application.

4:30 PM - 4:55 PM
2.7 High-performance (EOT<0.4nm, Jg~10-7A/cm2) ALD-deposited RuSrTiO3 stack for next generations DRAM pillar capacitor (Late News), *M. Popovici, A. Belmonte, H. Oh, G. Potoms, J.Meersschaut, O. Richard, H. Hodi, S. Van Elshocht, R. Delhougne, L. Goux, and G. Sankar Kar, imec*

We demonstrate the fabrication of strontium titanate (STO) based metal-insulator-metal (MIM) capaci tors with very-high dielectric constant (k~118) and low leakage of 10-7 A/cm2 at +/-1V for a ~11nm thick dielectric using Ru as bottom electrode (BE) and top electrode (TE). The k enhancement is attributed to the formation of an ultrathin cubic SrRuO3 phase at the RuSTO bottom interface, acting as a template optimizing the STO crystal quality from the interface to the bulk. This interface quality is evidenced by the same k~118 extracted from STO thickness series and relating to the bulk-k value. This achievement opens up an alternative integration roadmap for DRAM capacitors, moving from the current cup-shape to a denser pillar-shape design.