Session 13: Nano Device Technology - Nano-Devices for Low-Power Technologies
Tuesday, December 4, 9:00 AM
Continental Ballroom 4
Co- Chairs: L-E Wernersson, Lund University
W. Zhu, University of Illinois at Urbana-Champaign

9:05 AM - 9:30 AM
13.1 ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing, *J. Tang, D. Bishop, S. Kim, M. Copel, T. Gokmen, T. Todorov, S Shin, K-T Lee, P. Solomon, K. Chan, W. Haensch, J. Rozen IBM TJ WatsonResearch*

We have demonstrated a nonvolatile ECRAM that relies on electrochemically driven Li-ion intercalation for neuromorphic computing. It shows near-ideal switching symmetry and linearity, large dynamic range, up to 1000 discrete conductance states, and excellent endurance. Most importantly, sub-10 ns programming and sub-micron devices are both demonstrated for the first time.

9:30 AM - 9:55 AM
13.2 SoC Logic Compatible Multi-Bit FeMFET Weight Cell for Neuromorphic Applications, *K. Ni, J. A. Smith, B. Grisafe, T. Rakshit*, B. Obradovic*, J. A. Kittl*, M. Rodder* and S. Datta*
*University of Notre Dame, Notre Dame, *Samsung Advanced Logic Lab*

We demonstrate an SoC logic compatible ferroelectric-metal field effect transistor (FeMFET) digital 2-bit weight cell by monolithic BEOL integration of a ferroelectric (FE) capacitor with the gate of a conventional Si HK/MG MOSFET. Through optimization of the area ratio between the FE capacitor and the MOSFET, we show: 1) program/erase write voltages can be scaled down to logic compatible level, ±1.8 V, simplifying write circuitry; 2) write speed of 100ns; 3) write endurance $>10^{10}$ cycles without degradation due to elimination of charge trapping in FE; 4) 2 bits/cell achieving software levels of accuracy for inference on MNIST training database; 5) state retention approaching 10^4 s for a depolarization field of 0.3 MV/cm; 6) Multi-port (independent read and write) operations.

9:55 AM - 10:20 AM
13.3 Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering, *Z. Wang, B Crafton, J. Gomez*, R. Xu**, A. Luo**, Z. Krivokapic***, L. Martin**, S. Datta*, A. Raychowdhury, A. Islam Khan, Georgia Institute of Technology, *University of Notre Dame, **University of California, ***Lawrence Berkeley National Laboratory*

We report the first experimental demonstration of ferroelectric field-effect transistor (FEFET) based spiking neurons. A unique feature of the ferroelectric (FE) neuron demonstrated herein is the availability of both excitatory and inhibitory input connections in the compact 1T-1FEFET structure, which is also reported for the first time for any neuron implementations. Such dual neuron functionality is a key requirement for bio-mimetic neural networks and represents a breakthrough for implementation of the third generation spiking neural networks (SNNs)—also reported herein for unsupervised learning and clustering on real world data for the first time. The key to our demonstration is the careful design of two important device level features: (1) abrupt hysteretic transitions of the FEFET with no stable states therein, and (2) the dynamic tunability of the FEFET hysteresis by bias conditions which allows for the inhibition functionality. Experimentally calibrated, multi-domain Preisach based FEFET models were used to accurately simulate the FE neurons and project their performance at scaled nodes. We also implement an SNN for unsupervised clustering and benchmark the network performance across analog CMOS and emerging technologies and observe (1) unification of excitatory and inhibitory neural connections, (2) STDP based learning, (3) lowest reported power (3.6nW) during classification, and (4) a classification accuracy of 93%.

10:20 AM - 10:45 AM

13.4 Near Hysteresis-Free Negative Capacitance InGaAs Tunnel FETs with Enhanced Digital and Analog Figures of Merit below VDD=400mV, *A. Saeidi, A. S. Verhulst*, I. Stolichnov, A. Alian*, H. Iwai**, N. Collaert*, and A. M. Ionescu, EPFL, *imec, **Tokyo Institute of Technology*

We report the universal boosting impact of a true negative capacitance (NC) effect on digital and analog performances of Tunnel FETs (TFETs), mirrored for the first time in near hysteresis-free experiments and exploiting the S-shaped polarization characteristics. Well behaved InGaAs planar TFETs with a minimum swing of 55 mV/dec at room temperature are combined with high-quality single crystalline PZT capacitors, placed in series with the gate. When fully satisfying the exact NC matching conditions by a single crystalline ferroelectric that can perform a mono-domain state, a hysteresis-free (sub-10 mV over 4 decades of current) NC-TFET with a sub-thermionic swing and an SSmin of 40 mV/dec is demonstrated for the first time. In other devices, improvement in the subthreshold swing, down to 30 mV/dec, and analog current efficiency factor, up to 150 V-1, are achieved in NC-TFETs with a hysteresis as small as 30 mV. Importantly, the I60 FoM of the TFET is improved up to 2 orders of magnitude. The supply voltage is thereby reduced by 50%, down to 300 mV, providing the same drive current. Our results show that NC can open a new direction as a universal performance booster in the FET design by significantly improving the low I60 and low overdrive of TFETs.

10:45 AM Coffee Break

11:10 AM - 11:35 AM

13.5 An Experimental Study of Heterostructure Tunnel FET Nanowire Arrays: Digital and Analog Figures of Merit from 300K to 10K, *T. Rosca, A. Saeidi, E. Memisevic*, L-E. Wernersson* and A.M.Ionescu, EPF Lausanne, *Lund University*

In this work, we experimentally report the figures of merit of state-of-the-art heterostructure Tunnel Field-Effect-Transistor (TFET) arrays from room (300K) down to cryogenic temperature (10K) at supply voltages below 400mV. We demonstrate here, for the first time, that InAs/InGaAsSb/GaSb Nanowire (NW) TFETs are robust enough to maintain excellent figures of merit over a large temperature range even in devices with a large number arrayed nanowires (here, from 4 to 184 nanowires per device), accounting for technological variability. The investigated Tunnel FETs have temperature-independent min and average subthreshold swings of 45mV/dec/67mV/dec in large NW arrays, versus ~36/45mV/dec in smaller arrays, once the trap-assisted tunneling is removed (from 150K down to 10K). In all NW arrays we observe improvement of the on-current and of maximum transconductance, gmax, at cryogenic temperatures, with very little dependence of temperature, from 150K to 10K. The paper reports that in the range 150K to 10K only band-to-band-tunneling dominates the analog figures of merit of Tunnel FETs; we measured transconductance efficiencincies higher than 60V-1 for small arrays (breaking the limit of CMOS at RT) and close to 42V-1 for large arrays, for supply volrages smaller than 100mV, offering the possibility to design future energy efficient readouts and analog-to-digital converters. In contrast with cryogenic MOSFETs, Tunnel FETs show almost no hysteresis (<24mV), steep transfer characteristics, are free of kinks in output characteristics, with a unique stability of the swing drift with T, and negligible threshold voltage drift in all arrays configurations.

11:35 AM - 12:00 PM

13.6 High thermal tolerance of 25-nm c-axis aligned crystalline In-Ga-Zn oxide FET, H. Kunitake, *K. Ohshima, K. Tsuda, N. Matsumoto, H. Sawai, Y. Yanagisawa, S. Saga, R. Arasawa, T. Seki, R. Tokumaru, T. Atsumi, K. Kato and S. Yamazaki, Semiconductor Energy Laboratory*

We developed FETs having gate lengths of 25 and 60 nm that are suited for high-temperature operation, using c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO) as its channel material. The FETs with a

gate length of 60 nm achieved off-state leakage currents of 10 zA at 150°C. Furthermore, cutoff frequency the FETs with a gate length of 25 nm was 33 GHz at room temperature and changing the temperature from room temperature to 150°C changed the cutoff frequency by only -13% against -36% in Si FET. The CAAC-IGZO FET enables integrated circuits that consume little power even under high-temperature environments.