Session 11: Process and Manufacturing Technology - Material and Processes for Advanced Silicon Technologies
Tuesday, December 4, 9:00 AM
Grand Ballroom A
Co- Chairs: S. Maitrejean, CEA-LETI
S. Ecoffey, University of Sherbrooke

9:05 AM - 9:30 AM
11.1 Conformal, Wafer-Scale and Controlled Nanoscale Doping of Semiconductors Via the iCVD Process, *J. H. Kim, H. K. Park, K. Y. Pak, A. Yoon*, Y. S. Kim*, S. G. Im, W. S. Hwang** and B. J. Cho, KAIST, *Lam Research Corporation, **Korea Aerospace University*

For the first time, a novel doping technique using an initiated CVD (iCVD) process was developed, facilitating the conformal, wafer-scale and controlled nanoscale doping of semiconductors at a high concentration. iCVD poly(boron allyloxide) (pBAO) and poly(triallyl phosphate) (pTAP) were used as a p-type and n-type dopant diffusion source, respectively. In detail, an optimized integration process was developed involving copolymer p(BAO-co-V3D3) passivation for pBAO and double-step deposition for pTAP. It was found that a dopant-containing polymer layer with a sub-10-nm thickness provided a high doping concentration at a shallow junction depth (10 nm) for both the p-type (10^{20} cm-3) and the n-type (10^{21} cm-3). Furthermore, the conformality and dopant distribution of the iCVD polymer layer were investigated using a high-aspect-ratio Si fin (5:1). The SOI nFET with iCVD doping at the source/drain regions exhibited better subthreshold swing and on-current values than a SOI nFET with conventional ion-implantation doping. Compared to other diffusion doping methods, the iCVD process could achieve lower sheet resistance.

9:30 AM - 9:55 AM
11.2 Low Temperature Sputtered Graphenic Carbon Enables Highly Reliable Contacts to Silicon, *M. Stelzer, M. Jung, U. Wurstbauer, A.W. Holleitner, and F. Kreupl, Technical University of* Munich

Titanium silicide (TiSi) contacts are commonly used metal-silicon contacts but are known to diffuse into the active region under high current stress. Recently we demonstrated that graphenic carbon (GC) deposited by CVD has the same low Schottky barrier on silicon as TiSi, but a much improved reliability against high current stress. The drawback of the CVD-GC is the required deposition temperature of ~ 900 °C. In this paper we demonstrate now that the deposition of graphenic carbon is possible at 100 - 400°C by a modified sputter process. We show that the sputtered carbon-silicon (SC-Si) contact is over 1 billion times more stable against high current stress pulses than the conventionally used TiSi-Si junction, while it has the same or even a lower Schottky barrier. Doping SC by nitrogen (CN) leads to an even lower resistivity and improved stability. The finding that there is a low temperature approach for using the superb carbon properties has important consequences for the reliability of contacts to silicon and opens up the use of GC in a plethora of other applications.

9:55 AM - 10:20 AM
11.3 Location-controlled-grain technique for monolithic 3D BEOL FinFET Circuits, *C-C Yang, T-Y Hsieh***, P-T Huang*, K-N Chen *, W-V Wu*, S-W Chen, C-H Chang, C-H Shen, J-M Shieh, C. Hu**, Meng-C Wu***, W-K Yeh, National Nano Device Laboratories, *National Chiao Tung University, **also with University of California, Berkeley, ***National Tsing Hua University*

A location-controlled-grain technique is presented for fabricating BEOL monolithic 3D FinFET ICs over SiO2. The grain-boundary free Si FinFETs thus fabricated exhibit steep sub-threshold swing (<70mV/dec.), high driving currents (n-type: 363 uA/um and p-type: 385 uA/um), and high Ion/Ioff (>10^6). According to simulation, the thickness of interlayer dielectric layer plays an important role and shall be thicker than

250nm for sequential pulse laser crystallization process to keep bottom device and interconnect at less than 400ºC

10:20 AM - 10:45 AM

11.4 Novel Materials and Processes in Replacement Metal Gate for Advanced CMOS Technology, *R. Bao, S. Hung*, M. Wang, K. Chung, S. Barman*, S. A Krishnan*, Y. Yang*, W. Tang*, L. Li*, Y. Lin*, M. S Chan*, Z. Chen*, X. Miao, M. Hopstaken, R. A Conti, H. Jagannathan, M. P Chudzik*, D. McHerron, B. S Haran, S. Natarajan*, IBM, *Applied Materials*

This paper addresses novel approaches at material and integration fronts for gate applications. Material wise, new n work function metal (WFM) material is explored to address the need for reducing gate resistance and maintaining proper Vt at 20Å or less WFM thickness. Integration wise, next generation dipole is tested with various process sequences to address the need in lowering overall thermal budget at the gate level for advanced architectures, such as scaled FinFET and Nanosheets.

10:45 AM Coffee Break

11:10 AM - 11:35 AM

11.5 Why GeO_2 growth on Ge is suppressed and GeO_2/Ge stack is much improved in high pressure O_2 oxidation?, *X. Wang and A. Toriumi, The University of Tokyo*

This paper reports for the first time a new kinetic model of thermal oxidation of Ge that considers both O-vacancy and atomic O diffusion as a function of O2 pressure. The model is based on newly obtained results that Ge oxidation is described by kinetics completely different from the Deal-Grove model and that it exhibits anomalous O2 pressure dependence. Furthermore, new experimental results have been obtained in the oxidation of SiO2/GeO2/Ge, GeO2/SiO2/Si and GeO2/SiO2/Ge stacks. They support new kinetic model of Ge oxidation as well. This is critically important for high quality Ge gate stacks, as the Deal-Grove model have played a considerable role in Si technology.

11:35 AM - 12:00 PM

11.6 EUV Lithography at Threshold of High-Volume Manufacturing (Invited), *A. Yen, ASML*

A throughput of >140 wph has been achieved on NXE:3400B EUV scanners at a source power of 250W. Power degradation rate has been concurrently driven down so that high system throughput can be maintained. Improvement in mask-area cleanliness has resulted in over 1,500 exposures per fall-on particle, and solid progress on the pellicle has been made.

12:00 PM - 12:25 PM

11.7 Half pitch 14 nm direct pattering with Nanoimprint lithography, *T. Nakasugi, T. Kono, K. Fukuhara, M. Hatano, H. Tokue, M. Komori, H. Tsuda,T. Komukai, K. Takahata, H. Kato, K. Kobayashi, A. Mitra, S. Kobayashi, S. Inoue, T. Higashiki, T. Motokawa*, M. Saito*, S. Kanamitsu*, M. Itoh*, T. Imamura**, K. Matasunaga**, K. Hashimoto**, Y. Kim***, J. Cho***, and W. Jung***, Toshiba Memory Corp, *Kawasaki, **Yokkaichi, Japan, ***SK hynix Inc.*

A half pitch 14 nm direct pattering is demonstrated by Nano-imprint lithography (NIL). A template, fabricated by a self-aligned double patterning on a mask-blanks-template, provides a resist pattern with smooth vertical sidewalls. It enables a 14 nm etched pattern. A NIL system NZ2C used for this experiment shows good performance.