2016 IEDM Short Course Schedule

Design and Technology Enablers for Computing Applications

Sunday, December 4, 2016
9:00 a.m. – 5:20 p.m.

Course Organizer: John Chen, NVIDIA

9:00 a.m. **Introduction and Overview**
John Chen, NVIDIA

9:15 a.m. **The Rise of Massively Parallel Processing**
Liam Madden, Xilinx

10:30 a.m. Break

10:45 a.m. **Interconnect Challenges for Computing,**
William J. Dally, NVIDIA

12:00 p.m. Lunch

1:15 p.m. **Breaking the Memory Bottleneck in Computing Applications with Emerging Memory Technologies: A Design and Technology Perspective,**
Michel Harrand and Gabriel Molas, CEA-Leti

2:05 p.m. **Breaking the Memory Bottleneck in Computing Applications – Part II: Device Level**
Gabriel Molas and Michel Harrand, CEA-Leti

3:00 p.m. Break

3:15 p.m. **PMICs for Computing…and how GaN Changes the Story**
Alberto Doronzo, Texas Instruments

4:05 p.m. **Advanced Packaging Technologies for System Integration**
Douglas Yu, TSMC R&D

5:20 p.m. **End Course**