2016 IEDM Short Course Schedule

Technology Options at the 5 Nanometer Node

Sunday, December 4, 2016
9:00 a.m. – 5:45 p.m.

Course Organizer: An Steegen, Imec

9:00 a.m. **Introduction and Overview**
An Steegen, Imec

9:15 a.m. **Patterning Technology for N5**
Akihisa Sekiguchi, Tokyo Electron Limited

10:30 a.m. Break

10:45 a.m. **Novel Channel Materials for High-Performance and Low-Power CMOS,**
Nadine Collaert, Imec

12:00 p.m. Lunch

1:15 p.m. **Options Beyond FinFETs at 5nm Node,**
Aaron Thean, National University of Singapore

2:15 p.m. Break

2:30 p.m. **Low Resistance Contacts to Enable 5nm Node Technology: Patterning, Etch, Clean, Metallization and Device Performance**
Reza Arghavani, Pan Yang, Kaihan Ashtiani, Harmeet Singh and Dave Hemker, Lam Research Corporation

3:30 p.m. **Parasitic R and C Mitigation Options for BEOl and MOL in 5 nm Node Technology**
Theodorous Standaert and Dan Edelstein, IBM

4:30 p.m. Break

4:45 p.m. **Metrology Challenges for 5nm Technology**
Ofer Adan, Applied Materials

5:45 p.m. **End Course**