



2024 IEDM Conference Theme
**Shaping Tomorrow's
Semiconductor Technology**



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2024 IEEE International Electron Devices Meeting

December 7-11, 2024

*Hilton San Francisco Union Square
San Francisco, California*

IEDM is pleased to announce increased
technical focus in the area of:

Advanced Logic Technology (ALT)

Topics

Papers are solicited in the following themes of interest:

- CMOS platform technologies & opportunities
- Logic device performance and circuit design challenges
- Advanced, novel process integration schemes and (applications-driven) scaling approaches
- Process module innovations and progresses in process control & process metrology
- Design technology co-optimization (DTCO), System technology co-optimization (STCO)

New or trending areas include:

- GAA (vertically stacked) nanosheets based devices and circuits; new channel materials
- Sequential, monolithic 3D integration, heterogenous chipllets, 2.5/3D integration, thermal management
- Logic for memory
- Interconnects (BEOL, Backside power delivery)
- BEOL compatible transistors

Paper Submission

Submission deadline: July 11th

Single submission of final, four-page paper